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Suzhou_UL

CPU : Intel Penryn
Chip Set : Intel Cantiga & ICH9M
Remarks : Montevina Platform

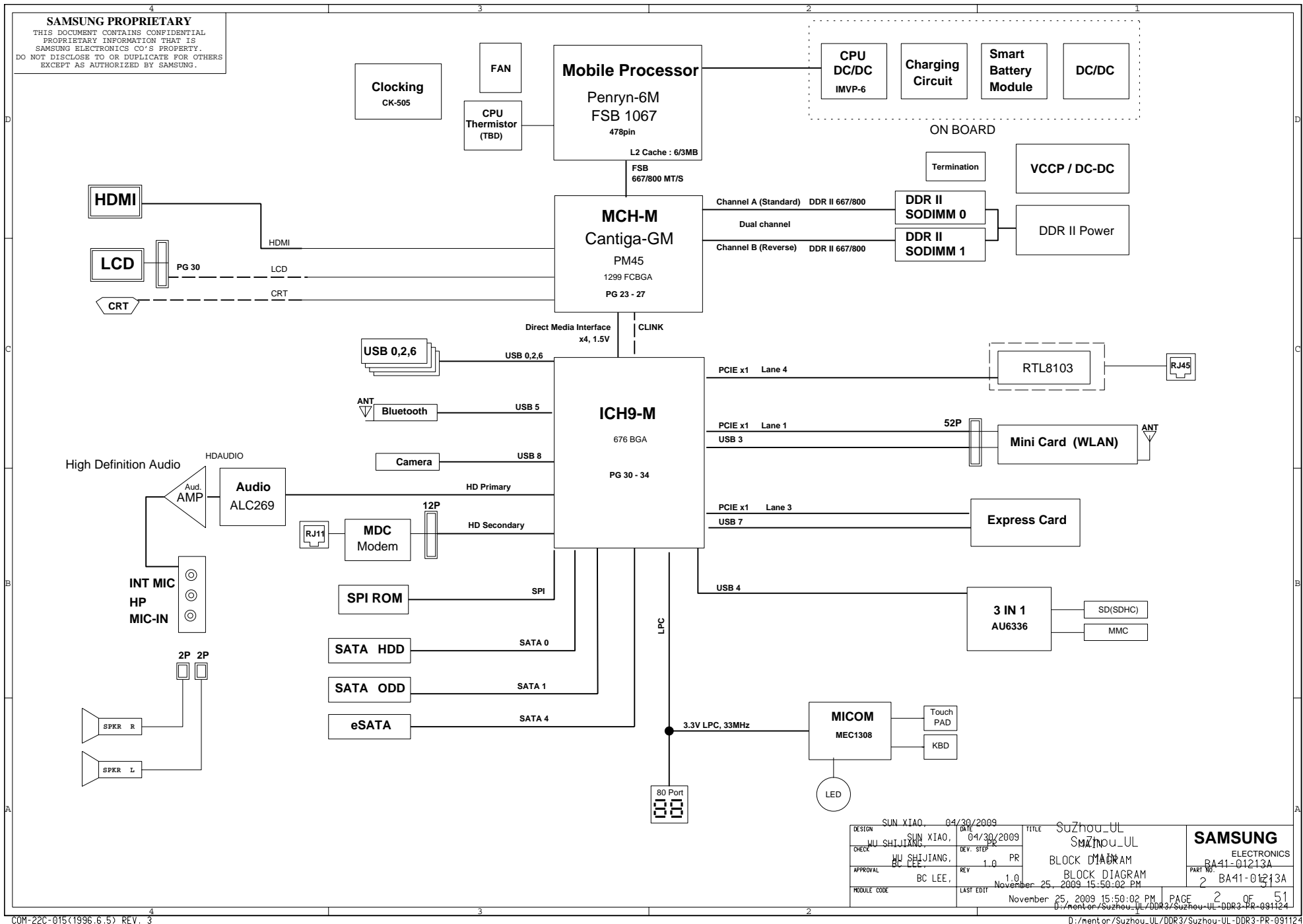
Model Name : Suzhou_UL_DDR3
PCB Code : GCE BA41-01213A
NAN BA41-01212A
HAN BA41-01214A

Dev. Step : P R
Revision : 1.0
T.R. Date : 2009.09.12

DESIGN	CHECK	APPROVAL

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0	COVER		
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM		PAGE	1 OF 51

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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (9 to 20V)
VCC_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	RealTek 88E8057

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

REVISION HISTORY

See rev notes for more information.

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	0	NC
1	SYSTEM PORT 1	1	Mini Card 1 (WLAN)
2	SYSTEM PORT 2	2	NC
3	NC	3	LOM
4	NC	4	Mini Card 2 (ROBSON or DVB-T)
5	Bluetooth	5	NC
6	Mini PCI Express 2		
7	Camera		
8	NC		
9	NC		

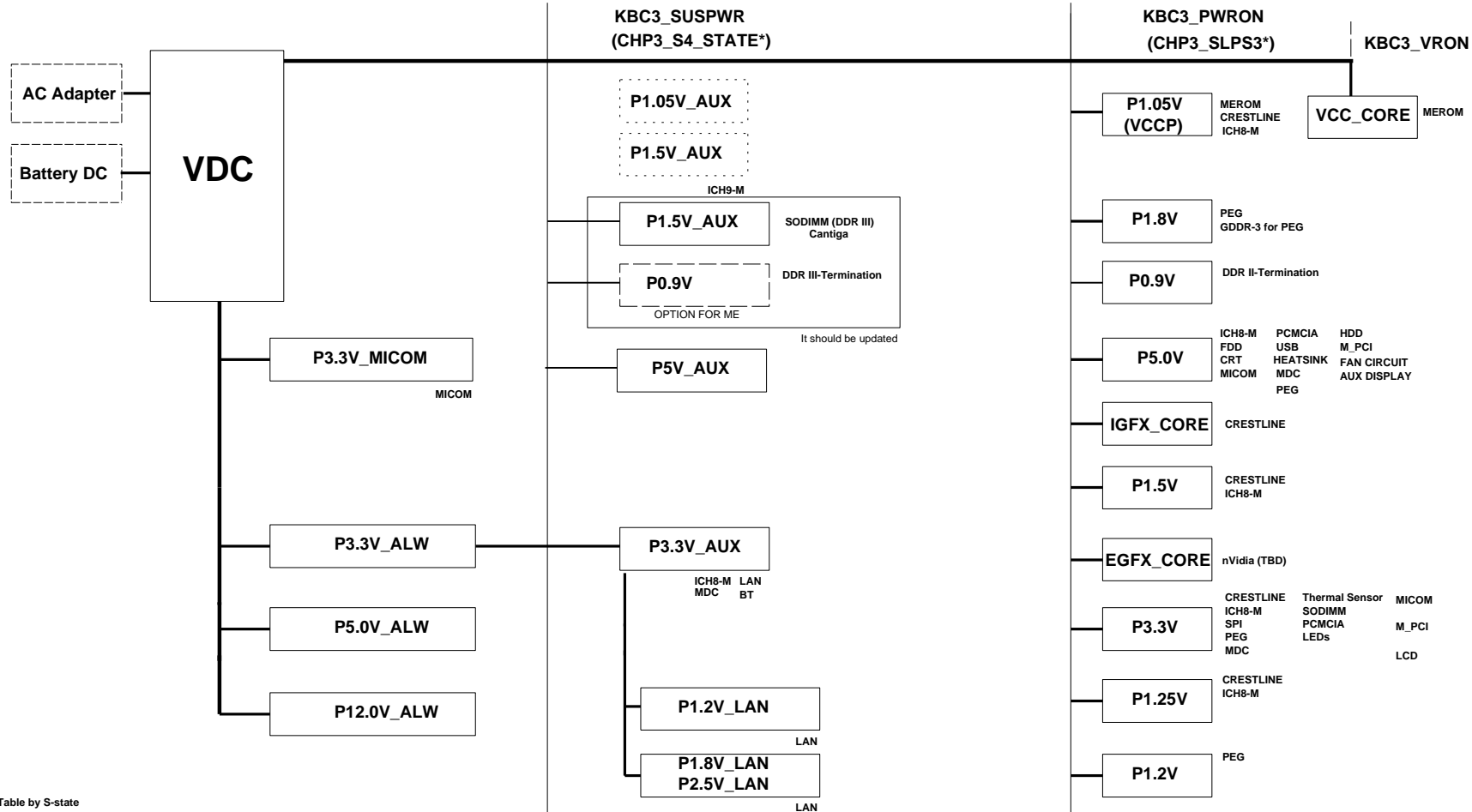
(This table will be update.)

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		MAIN	
APPROVAL	BC LEE,	REV	1.0		BCAFDINFO	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			
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POWER DIAGRAM

Rev 0.1



Power On/Off Table by S-state

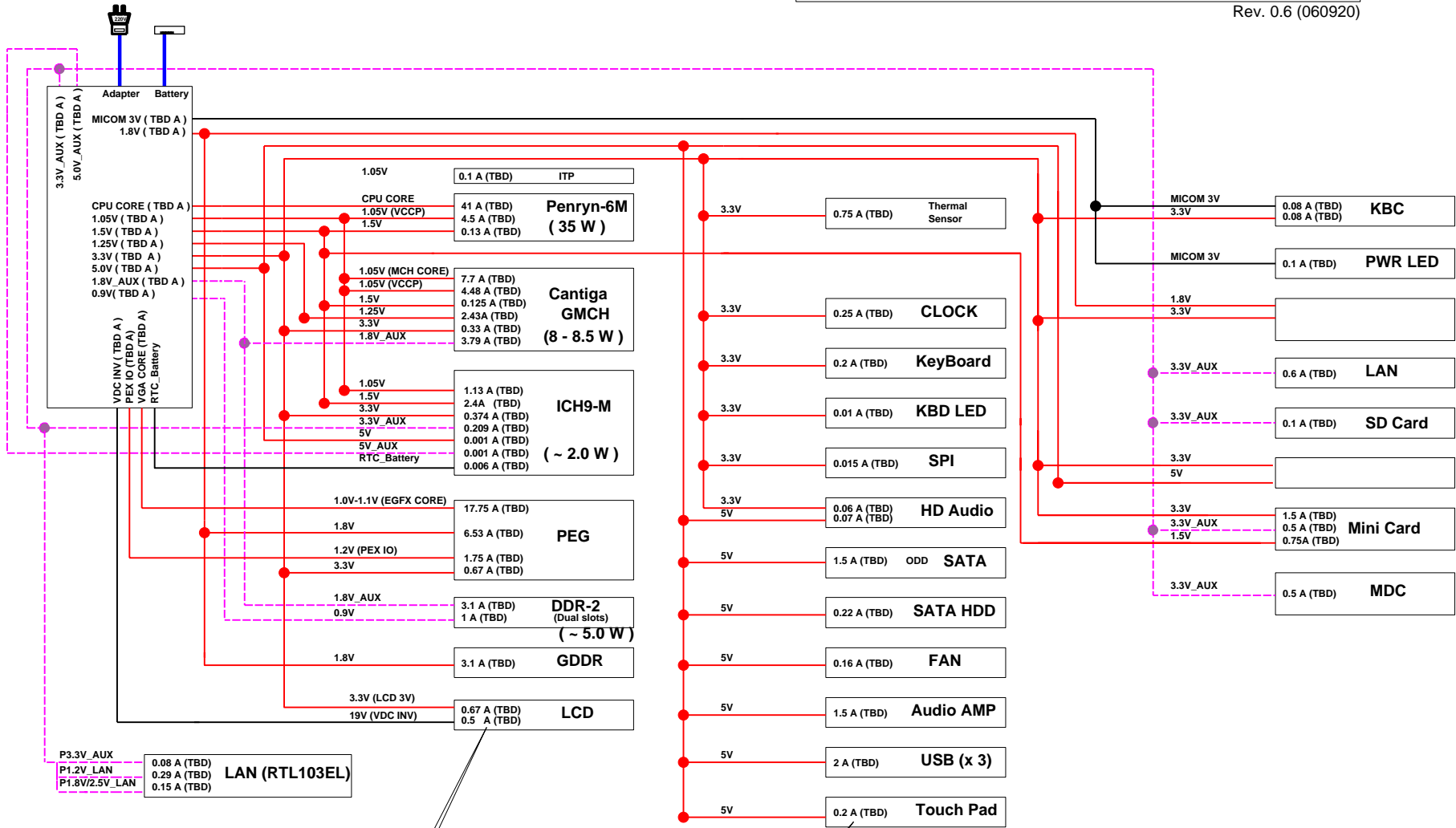
Rail	S0	S3	S4	S5
State	S0	S3	S4	S5
+V*(LWS)	ON	ON	ON	ON
+V*LAN	ON	ON	—	—
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		MAIN	
APPROVAL	BC LEE,	REV	1.0		POWER DIAGRAM	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	4 OF 51	

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POWER RAILS ANALYSIS

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

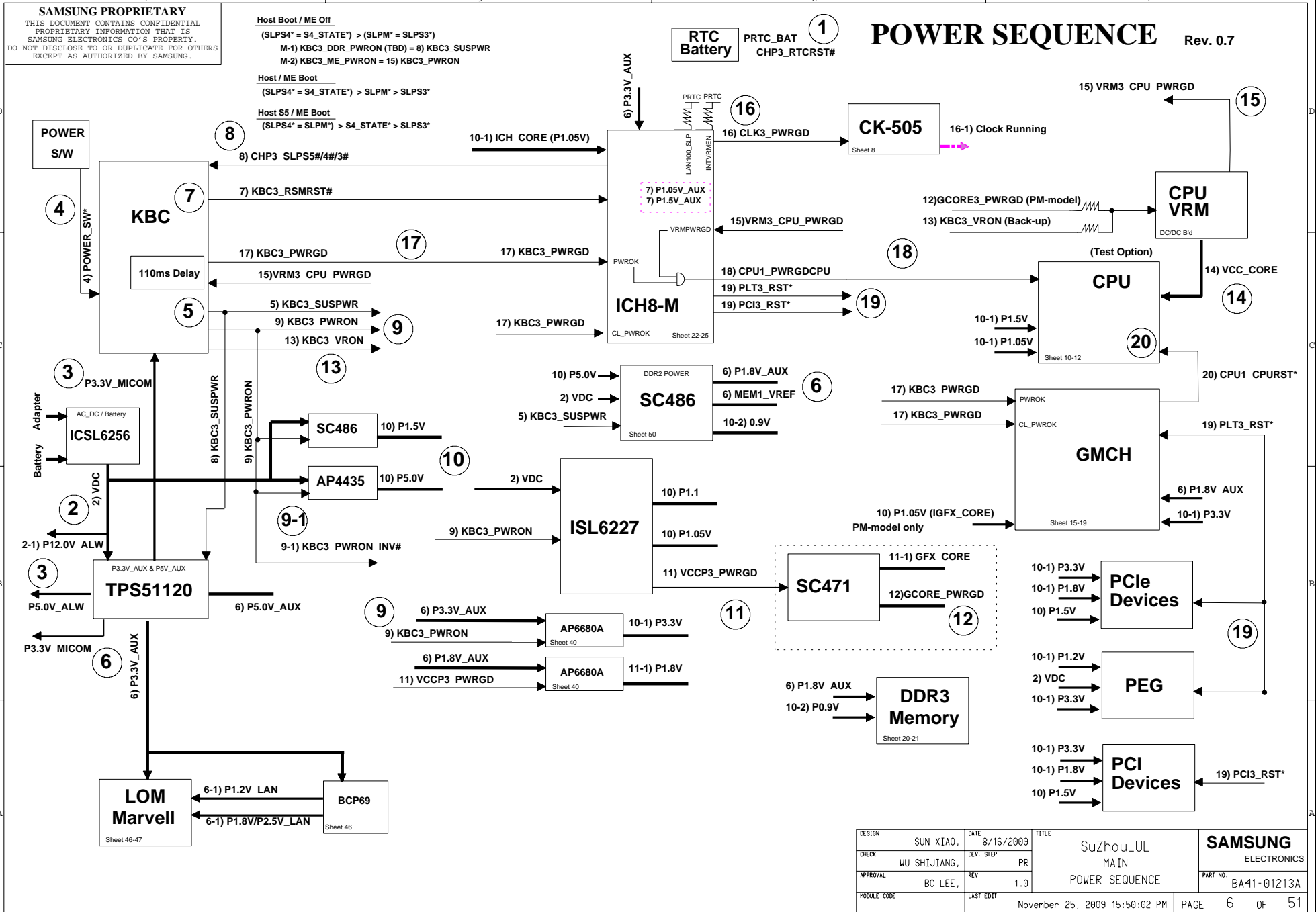
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CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN	POWER RAILS	
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	5	OF 51

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Host Boot / ME Off
(SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR
M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

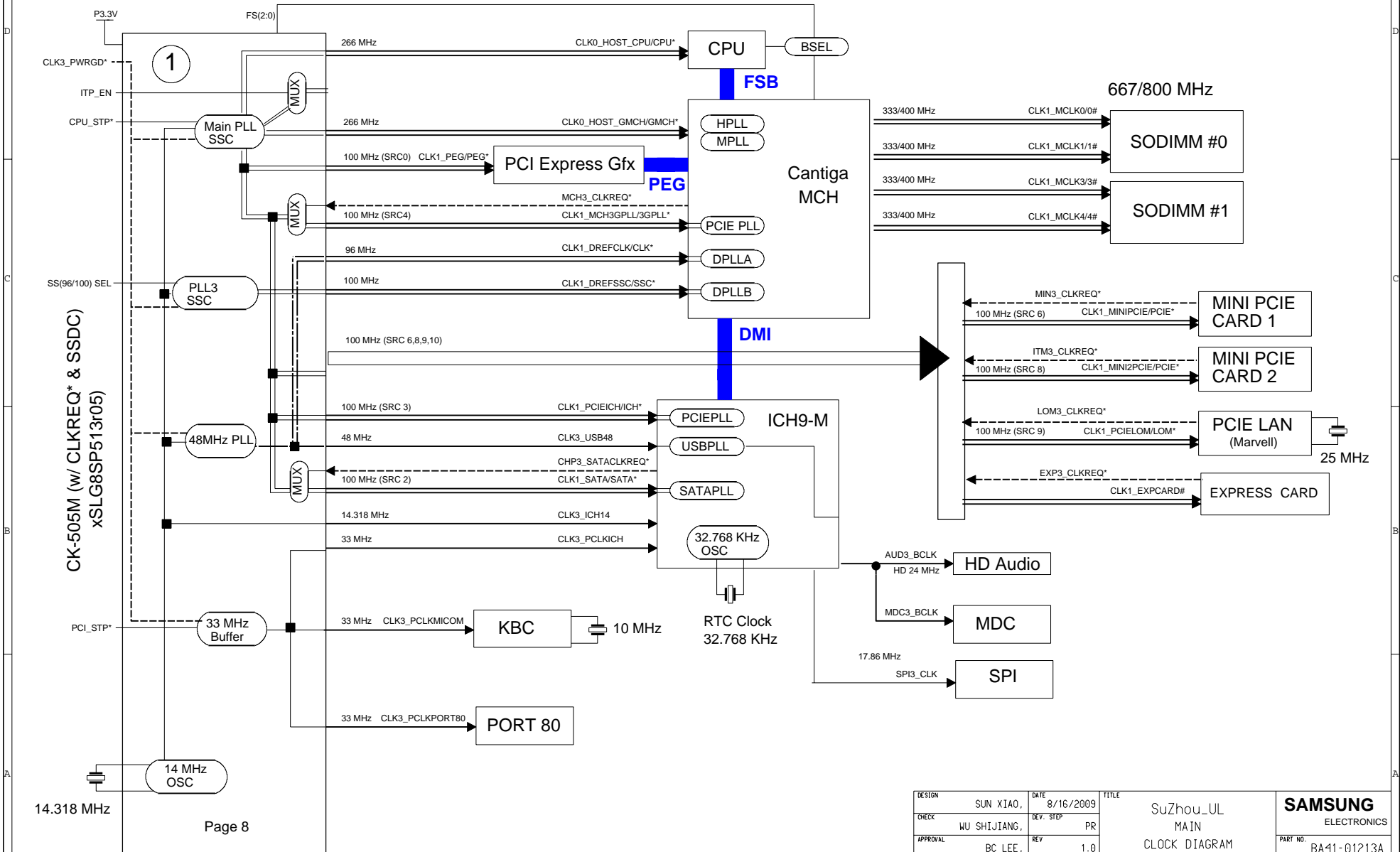
Host / ME Boot
(SLPS4* = S4 STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot
(SLPS4* = SLPM*) > S4 STATE* > SLPS3*



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CLOCK DISTRIBUTION Rev. 0.1

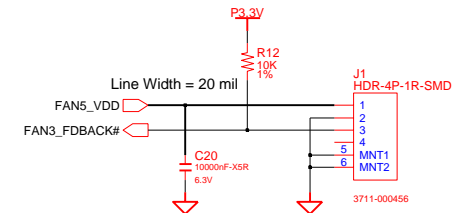
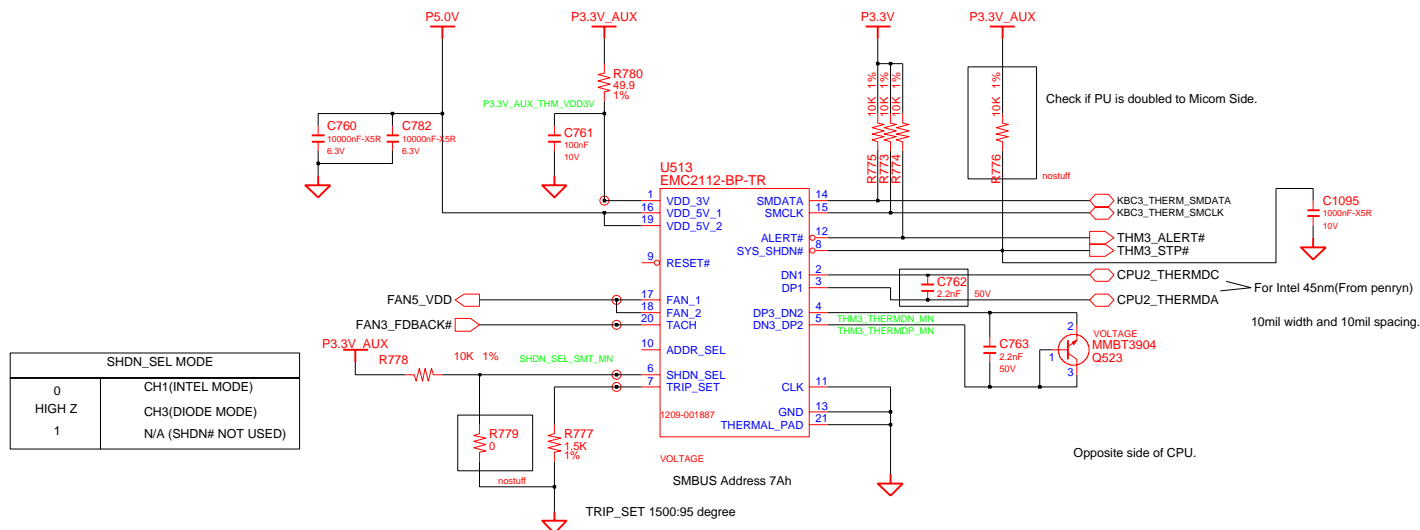


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DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	CLOCK DIAGRAM		
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			
PAGE 7 OF 51						PART NO. BA41-01213A

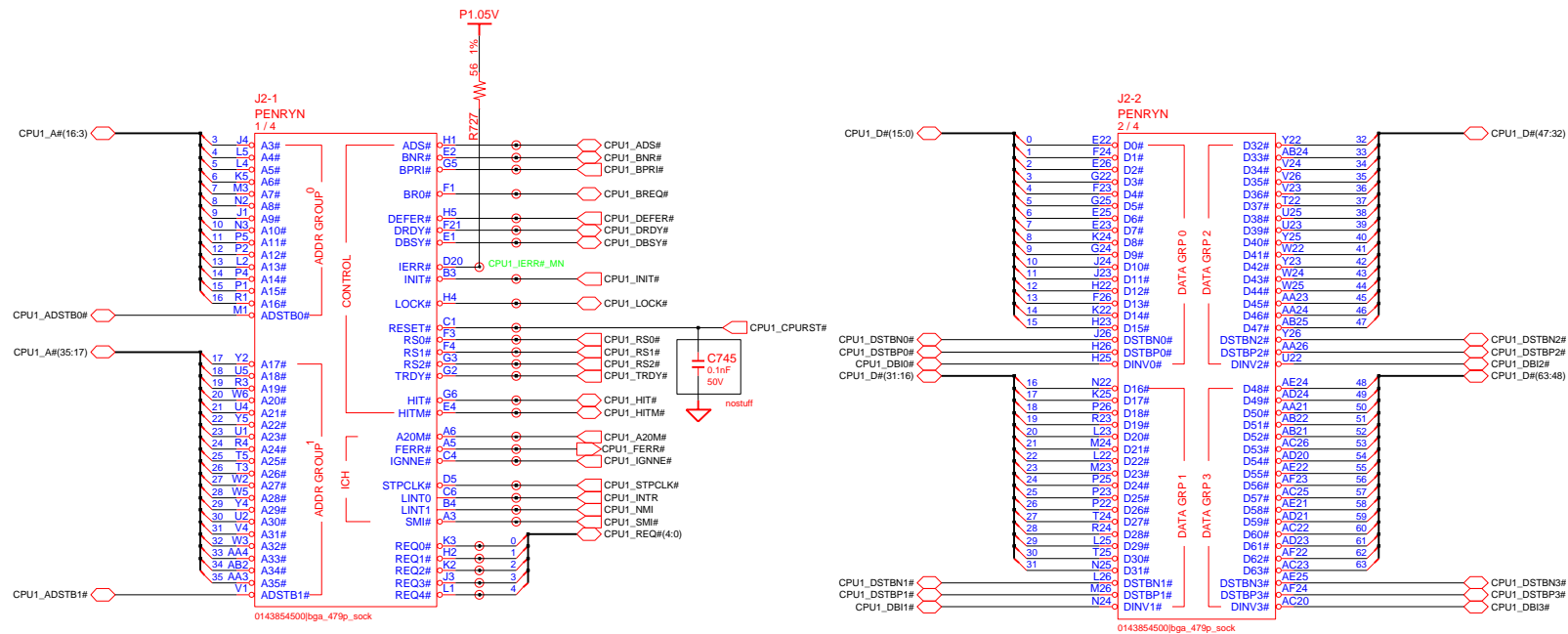
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THERMAL SENSOR & FAN CONTROL

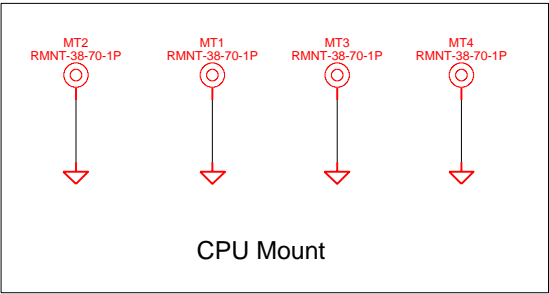


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CHECK	WU SHIJIANG,	DEV. STEP	PR		Thermal Sensor EMC2102	
APPROVAL	BC LEE,	REV	1.0			PART NO.
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			BA41-01213A
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CPU Socket: 3704-001153

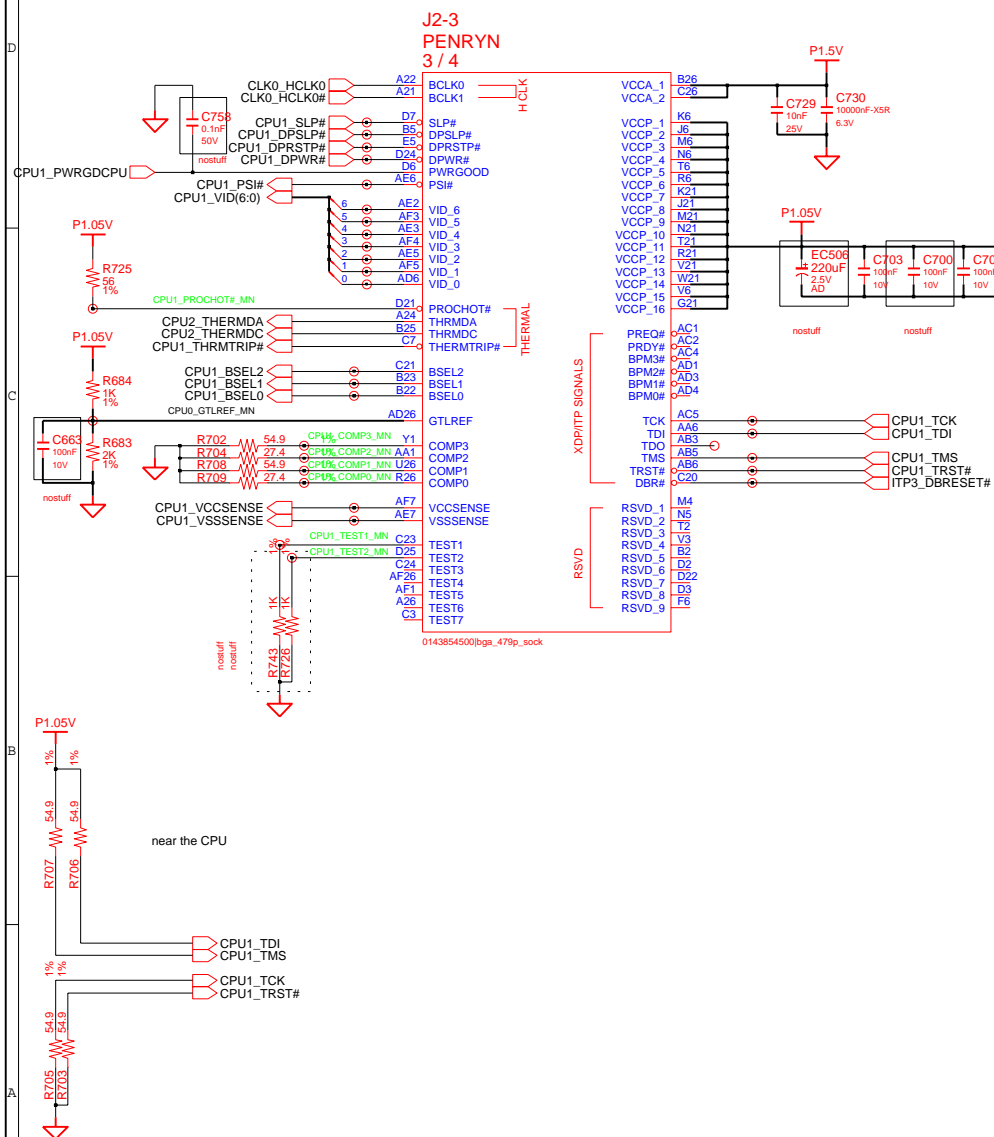


DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	SuZhou_UL
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APPROVAL	BC LEE,	REV	1.0	PENRYN (1/3)	
MODULE CODE	undefined	LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	9 OF 51

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PART NO. BA41-01213A

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CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 0	1.4875 V	0 1 1 0 0 0 0	0.9875 V	1 0 1 0 0 1 0	0.4800 V
0 0 0 0 0 0 1	1.4750 V	0 1 0 1 0 0 1	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 1 0 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 0 1	0.4300 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 0 1 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 0 1 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 0 1 1	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 0 0	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V

*Yonah Processor (2.33 GHz / 800 MHz : TBD)


GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with $Z_0=55\text{ohm}$ trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with $Z_0=27.4\text{ohm}(55\text{ohm})$ trace shorter than 1/2" to their respective Banias socket pins.

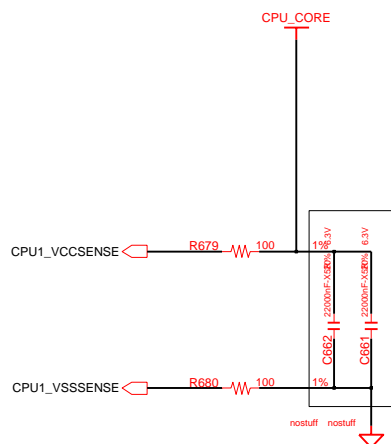
GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a $Z_0=55\text{ohm}$ traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

BSEL

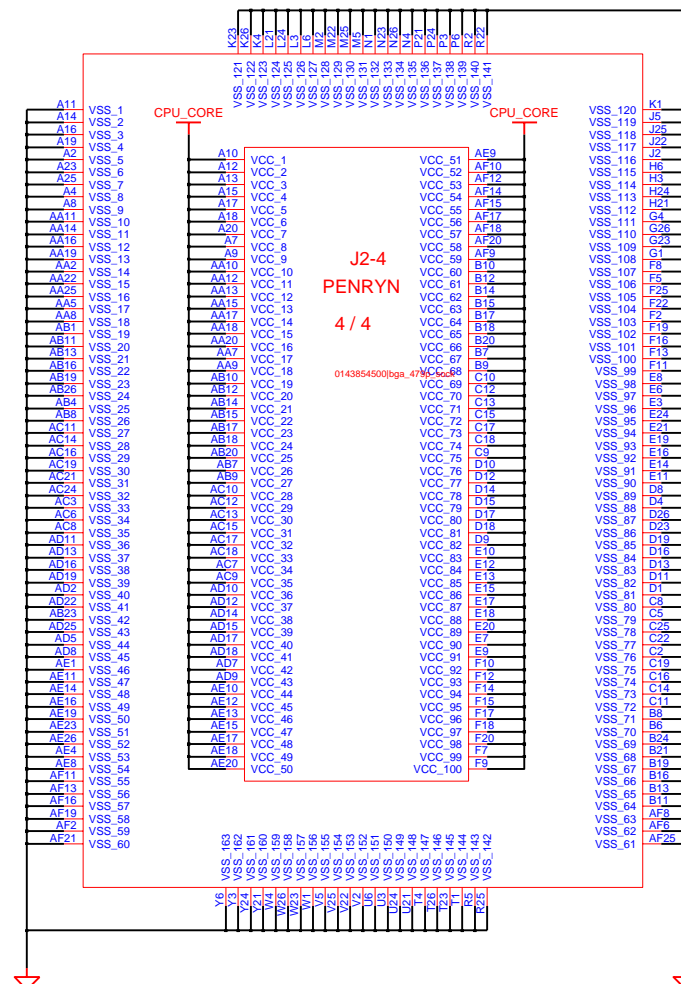
		Pull-down
FSB 1067 MHz		BSEL0, BSEL1, BSEL2
FSB 800 MHz		BSEL0, BSEL2


DATE	SUN XIAO,	11/8/2006	TITLE	SuZhou_UL CPU PENRYN (2/3)	
CHECK	WU SHIJIANG,	PR			
APPROVAL	BC LEE,	REV 1.0			
MODULE CODE	undef ined	LAST EDIT			

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6x 330 uF : CPU VR side



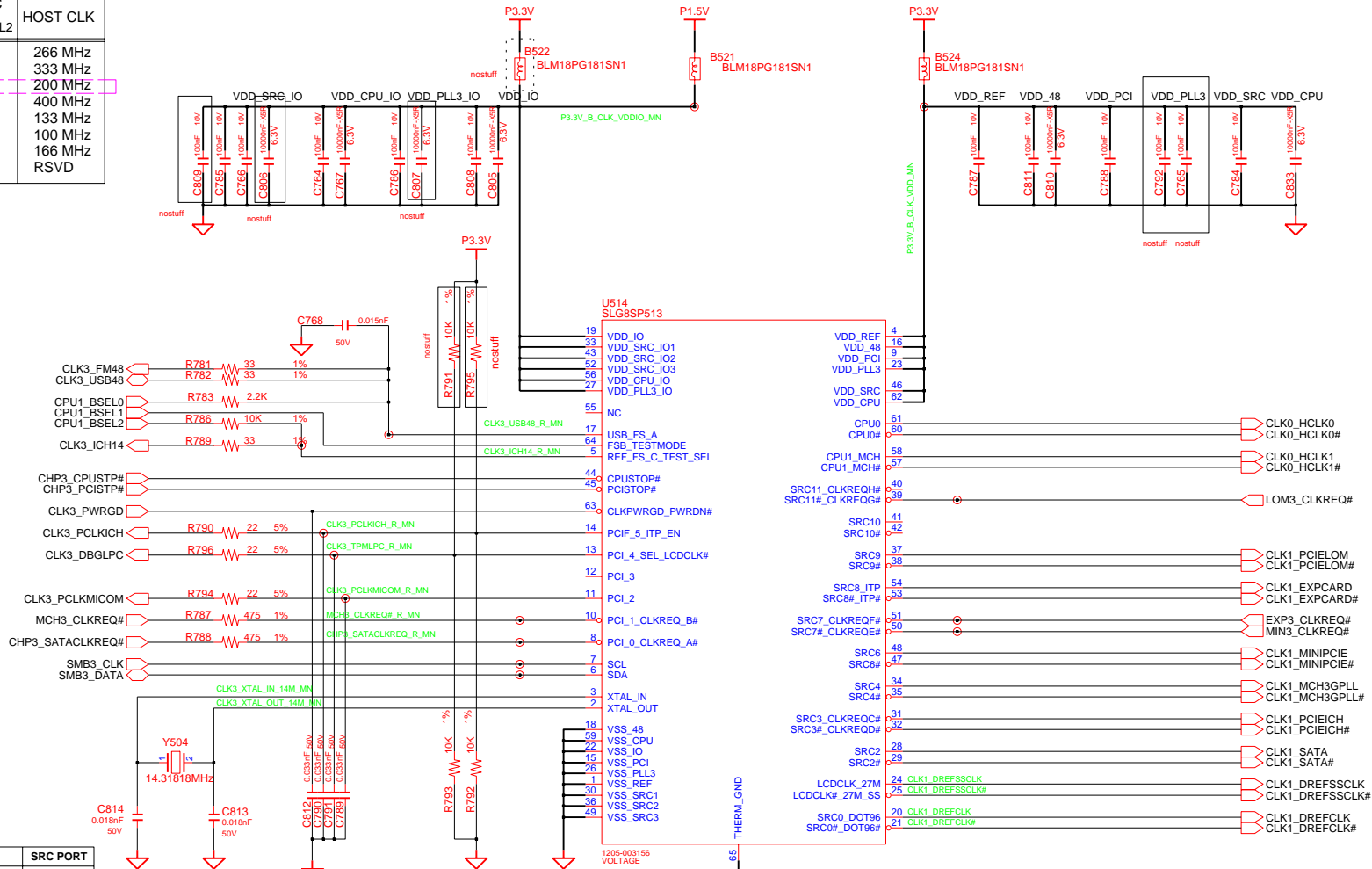
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CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT		November 25, 2009 15:50:02 PM		PAGE 11 OF 51

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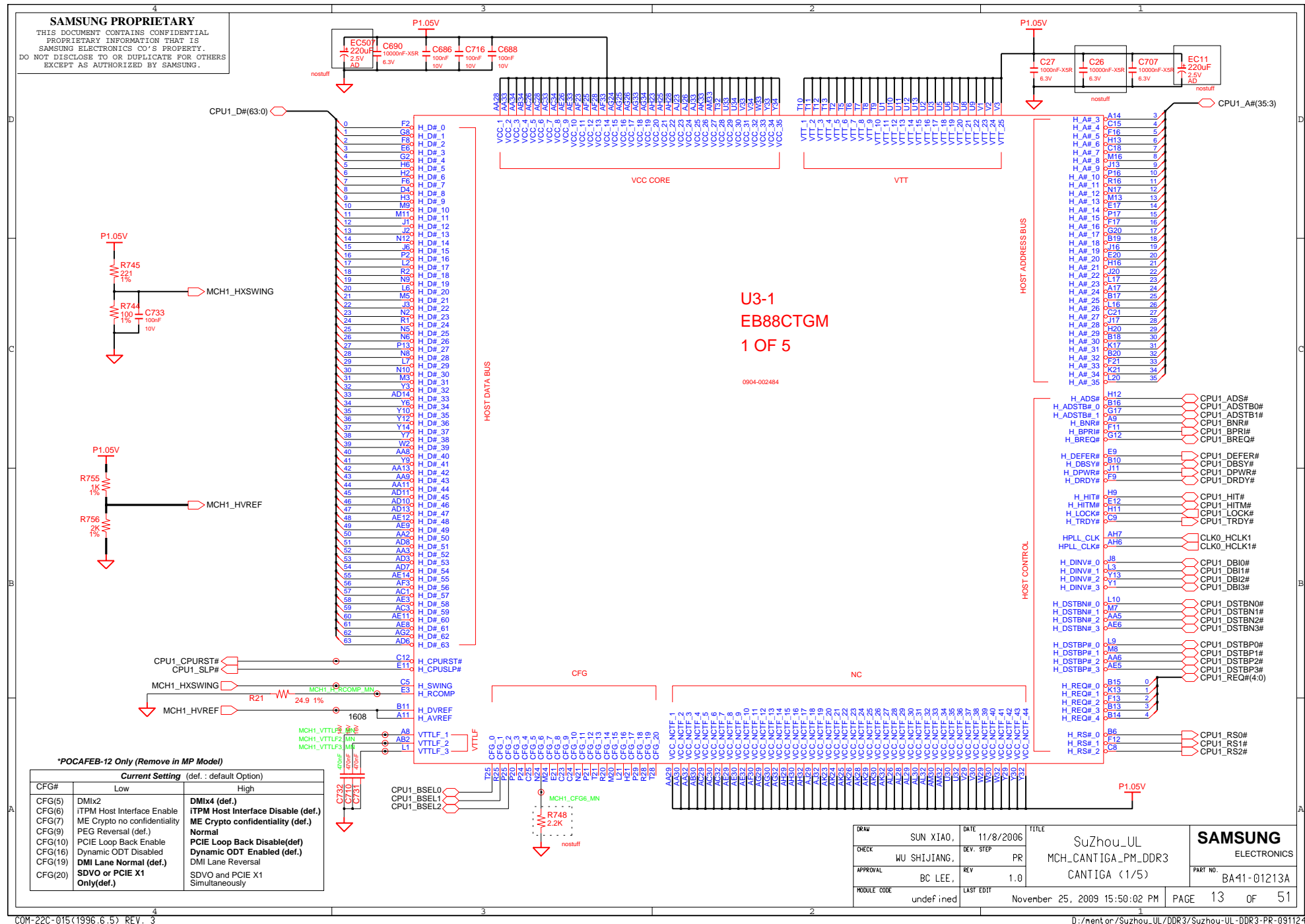
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CK505M

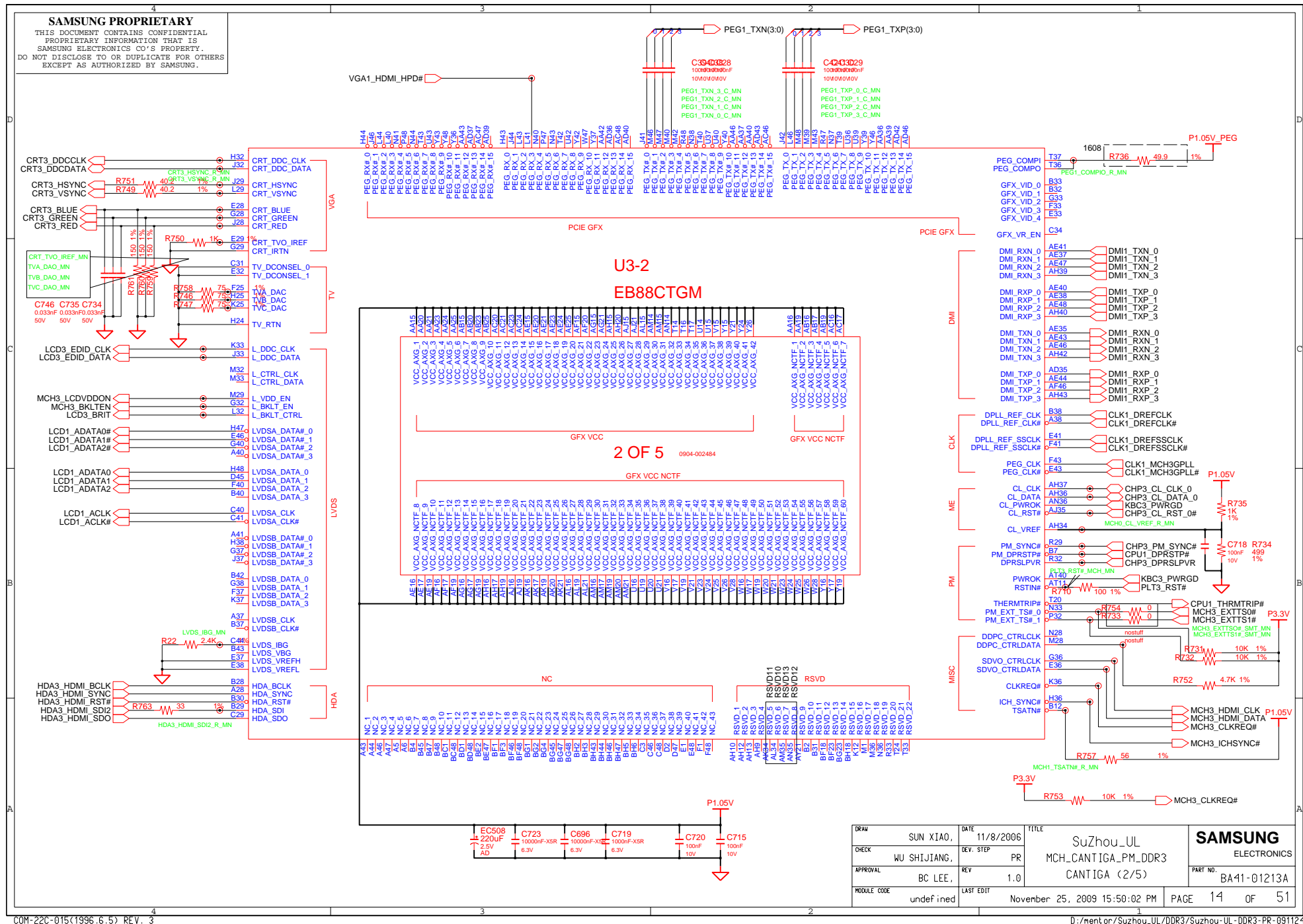
FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



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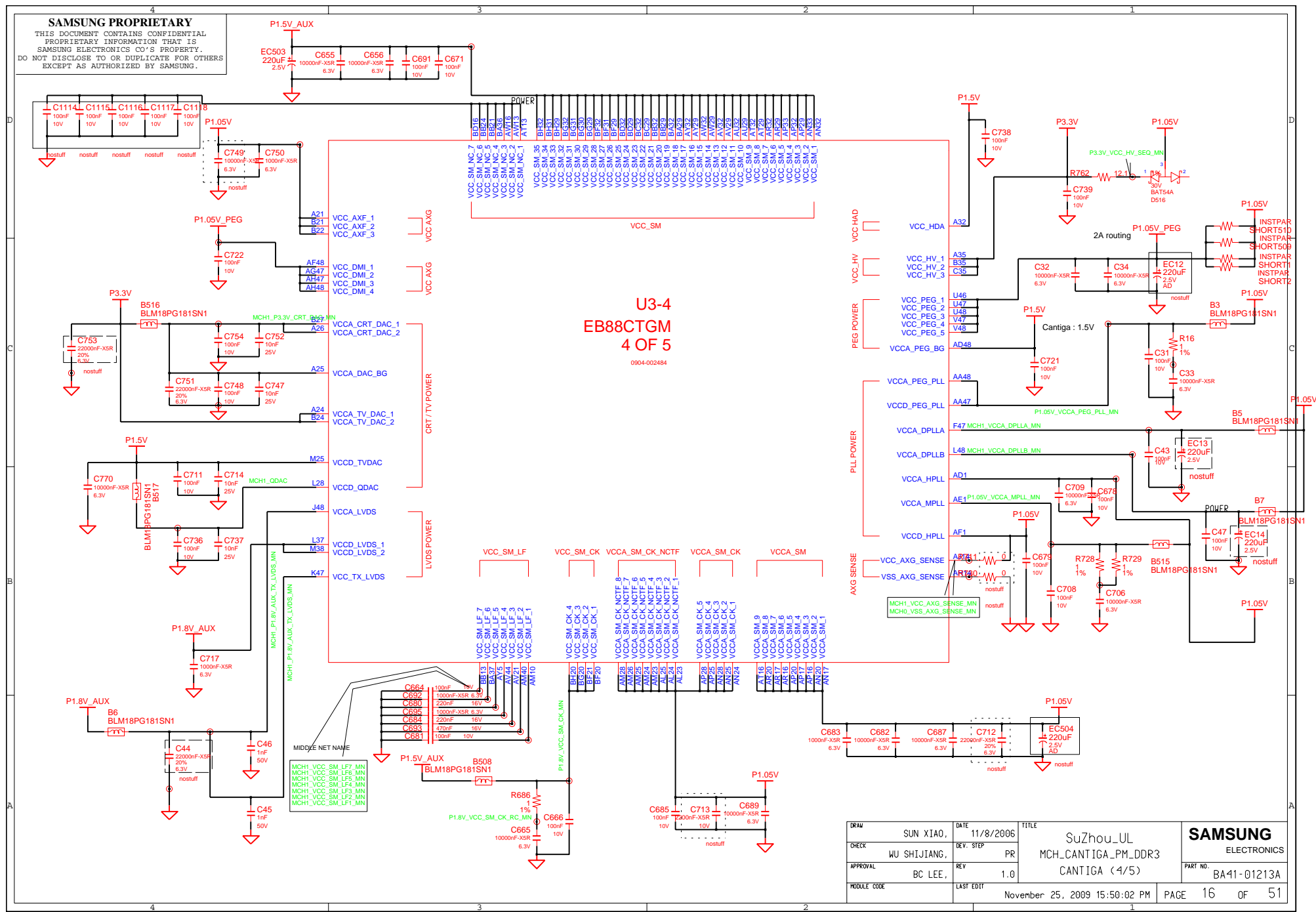
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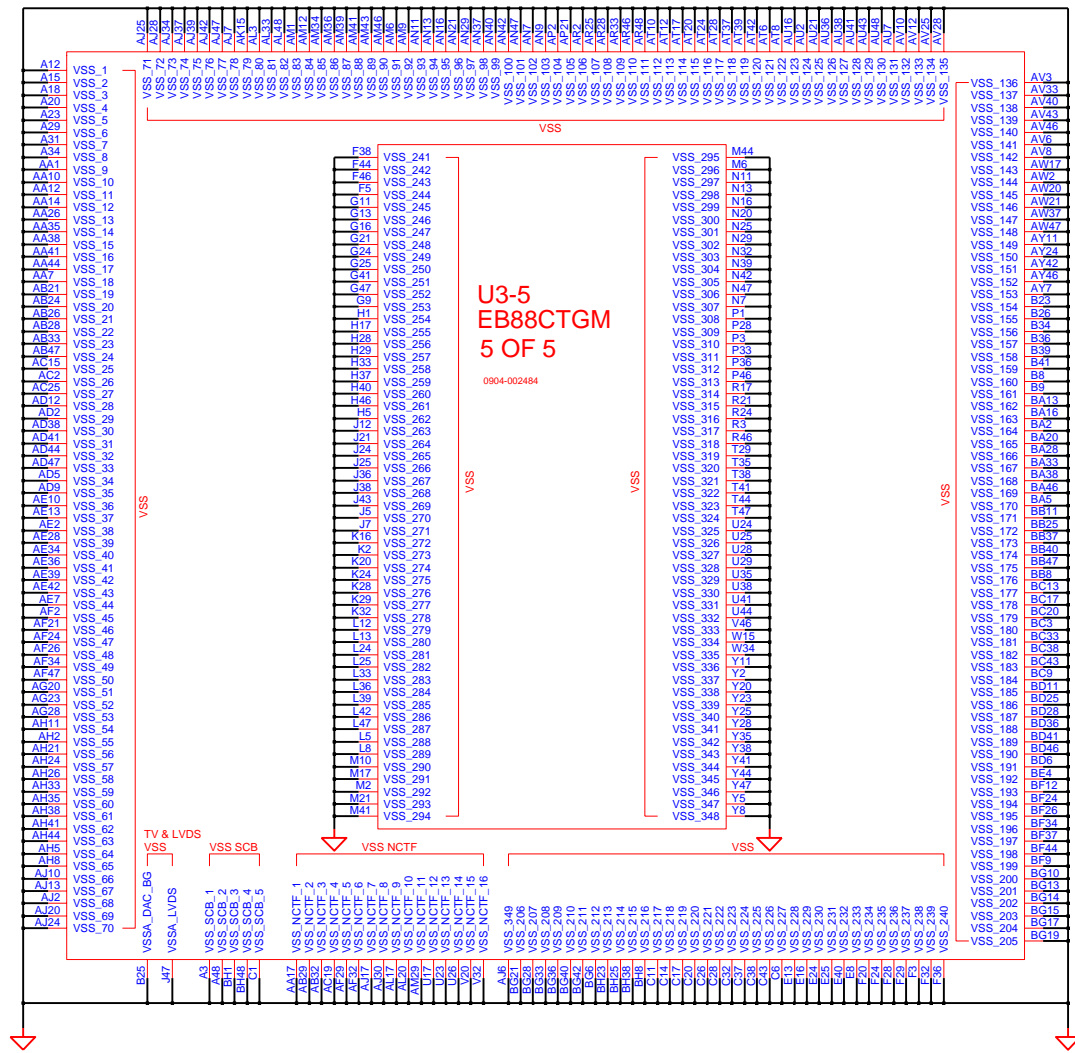
COM-22C-015(1996.6.5) REV. 3	3	2	1	D:\ment or\Suzhou-UL\DDR3\Suzhou-UL-DDR3-PR-09112
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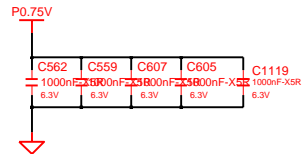
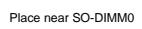


DATE	SUN XIAO,	11/8/2006	TITLE	SuZhou_UL	
CHECK	WU SHIJIANG,	DEV. STEP	PR	MCH_CANTIGA_PM_DDR3	
APPROVAL	BC LEE,	REV	1.0	CANTIGA (4/5)	
MODULE CODE		LAST EDIT		PART NO. BA41-01213A	

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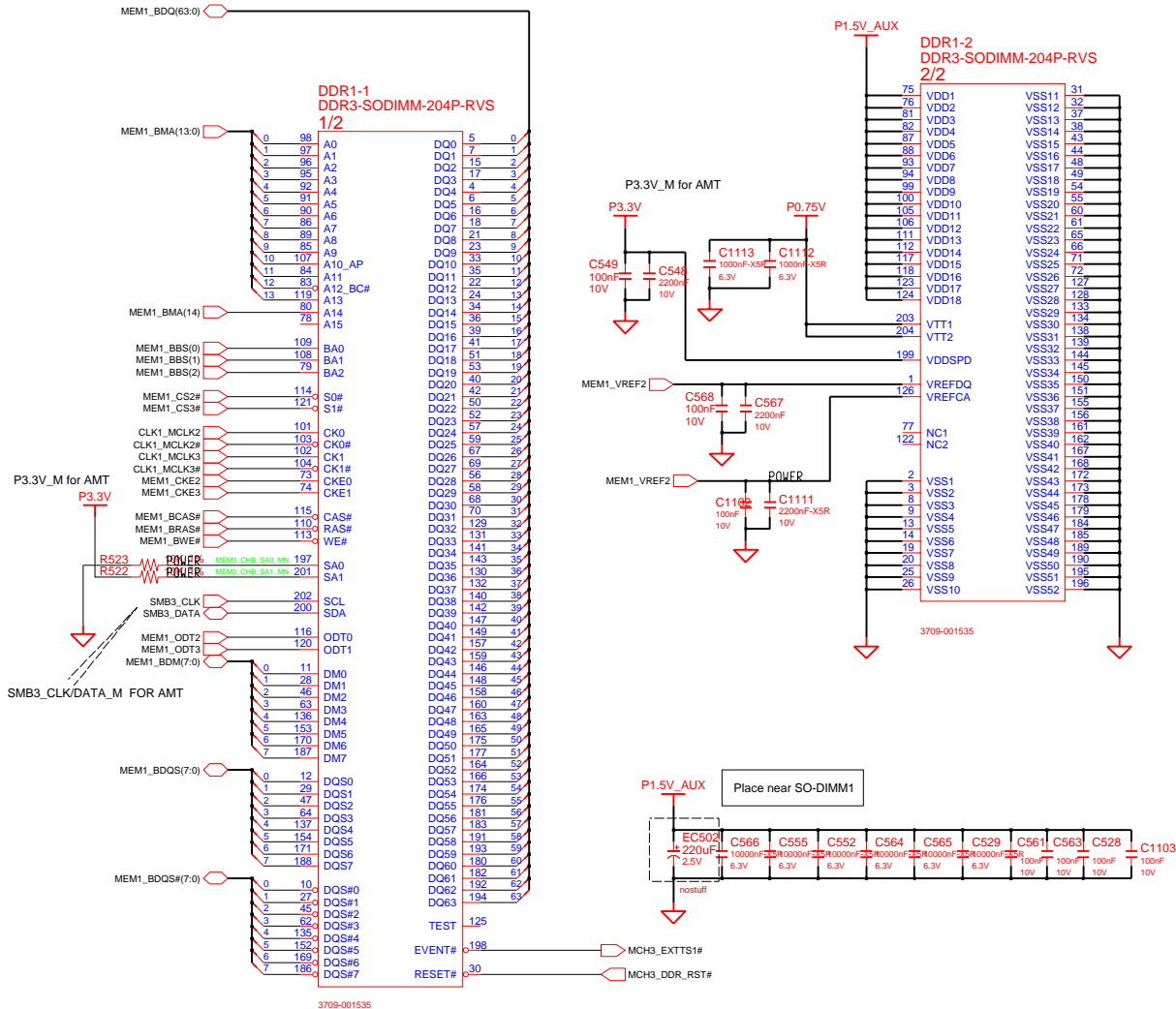
DDR SO-DIMM #0

D:/mentor/Suzhou_UL/DDR3/Suzhou-UL-DDR3-PR-091124

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DDR SO-DIMM #1

Array resistors & Single resistors used to improve layout & routing.

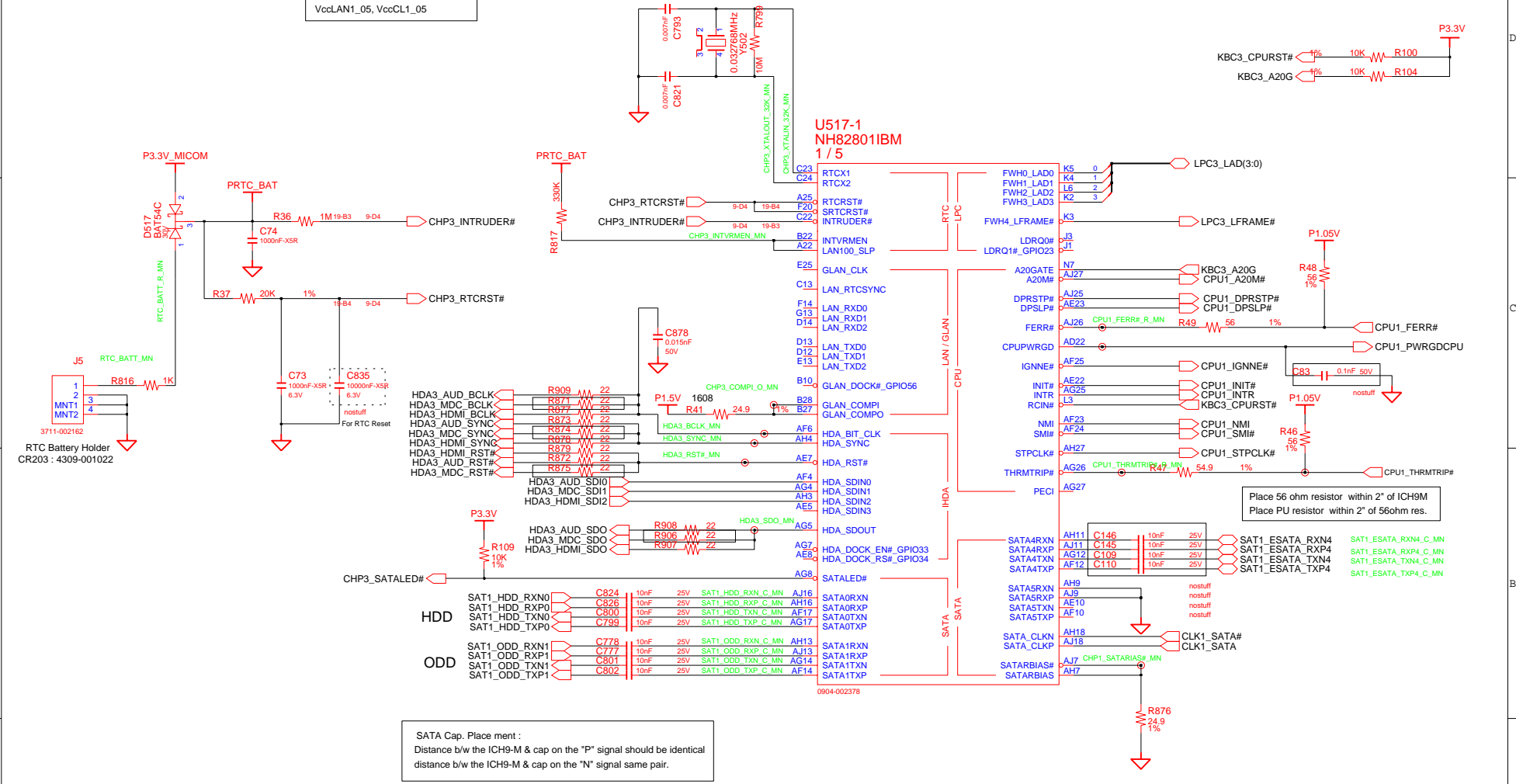


DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	SuZhou_UL
CHECK	WU SHIJIANG,	DEV. STEP	PR	SODIMM_REV	
APPROVAL	BC LEE,	REV	1.0	DDR3 CH B	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	19 OF 51

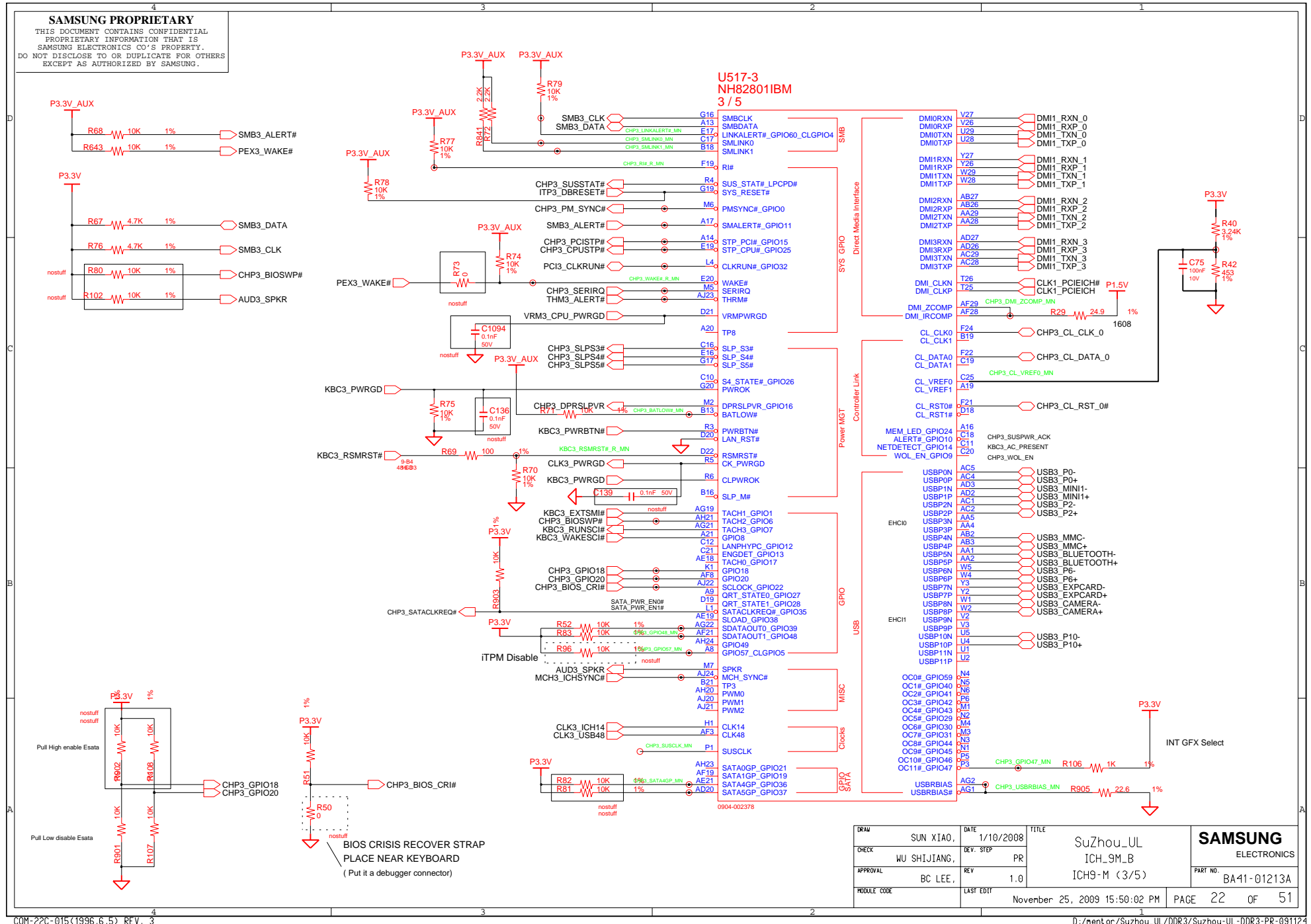
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Internal VR Strap
INTVRMEN Pull up
VccSus1_05, VccSus1_5, VccCl1_5
VccLAN1_05, VccCl1_05

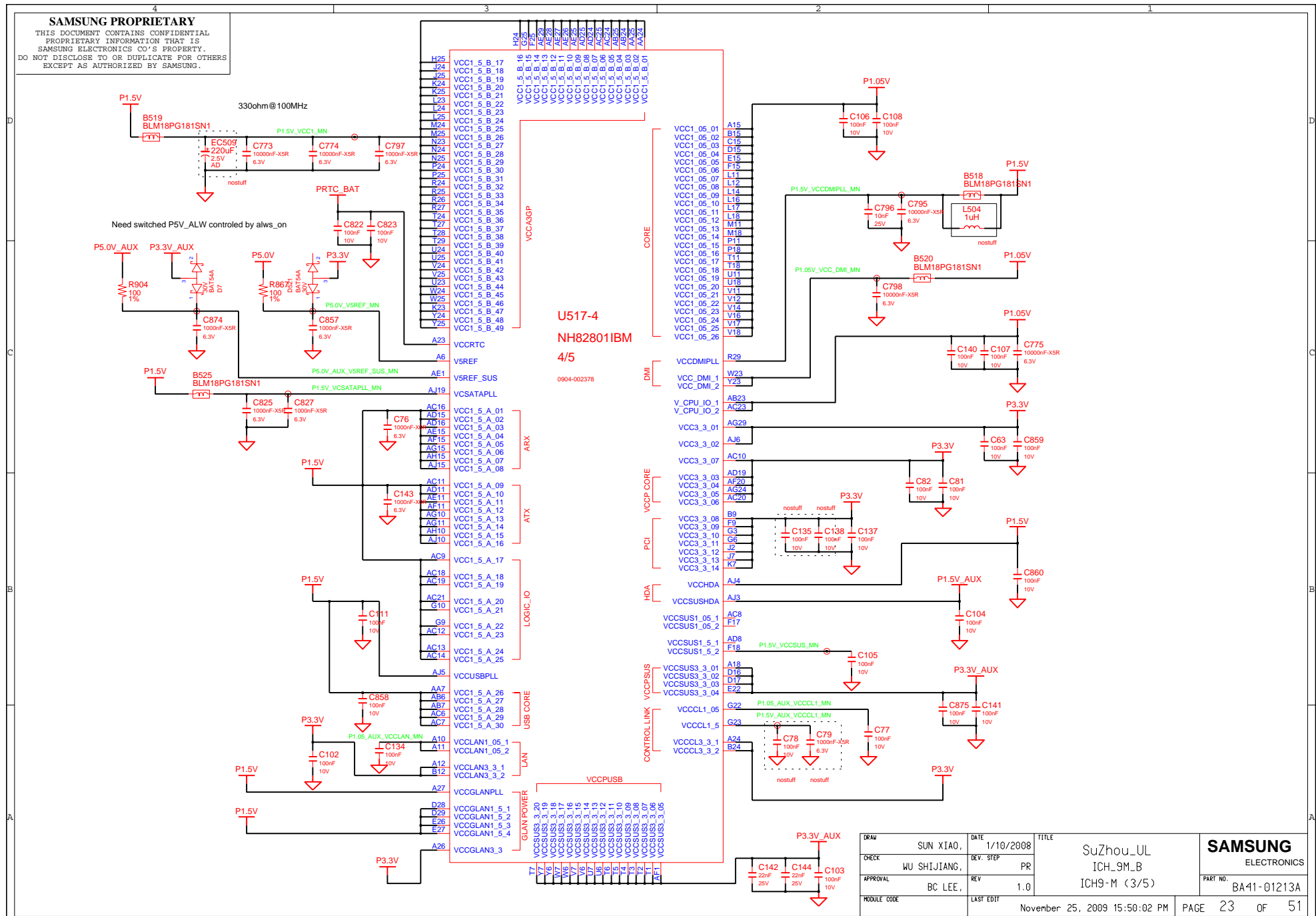


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ORAW	SUN XIAO,	DATE	1/10/2008	TITLE	SuZhou_UL ICH9M_B ICH9-M (3/5)	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE	LAST EDIT		November 25, 2009 15:00:02 PM			
					PAGE	22 OF 51

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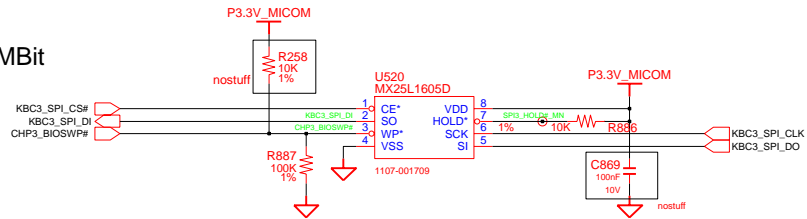


COM-22C-015(1996.6.5) REV. 3

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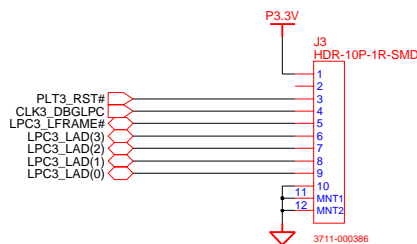
SPI_BIOS_ROM

16MBit

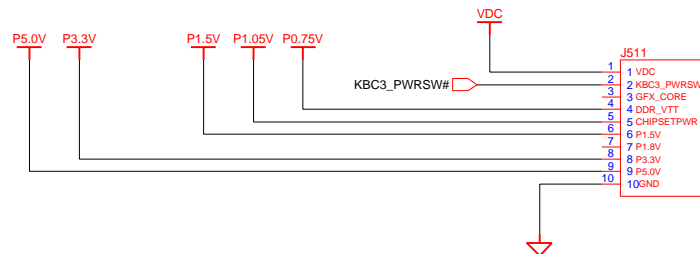


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
WITH INITIAL POST VALUE		88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	RESET CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	B8	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY PRESS SETUP	92	JUMP TO USER PATCH 1
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

80H DECODER CONNECTOR



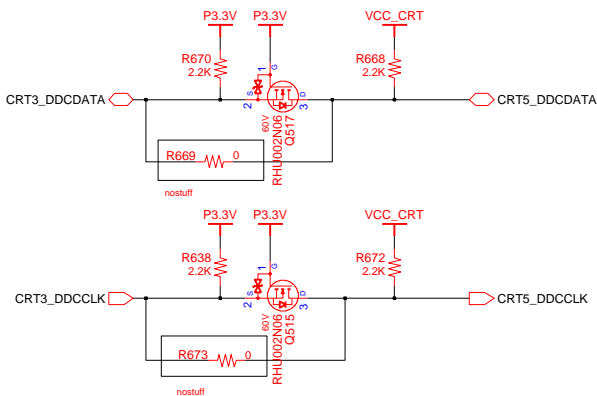
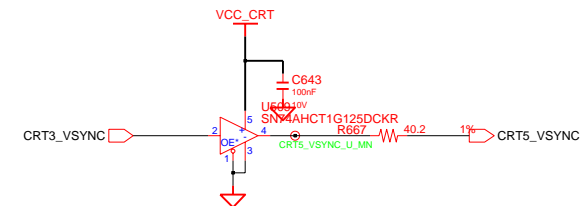
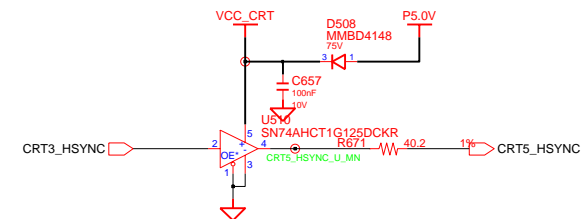
ICT PORT



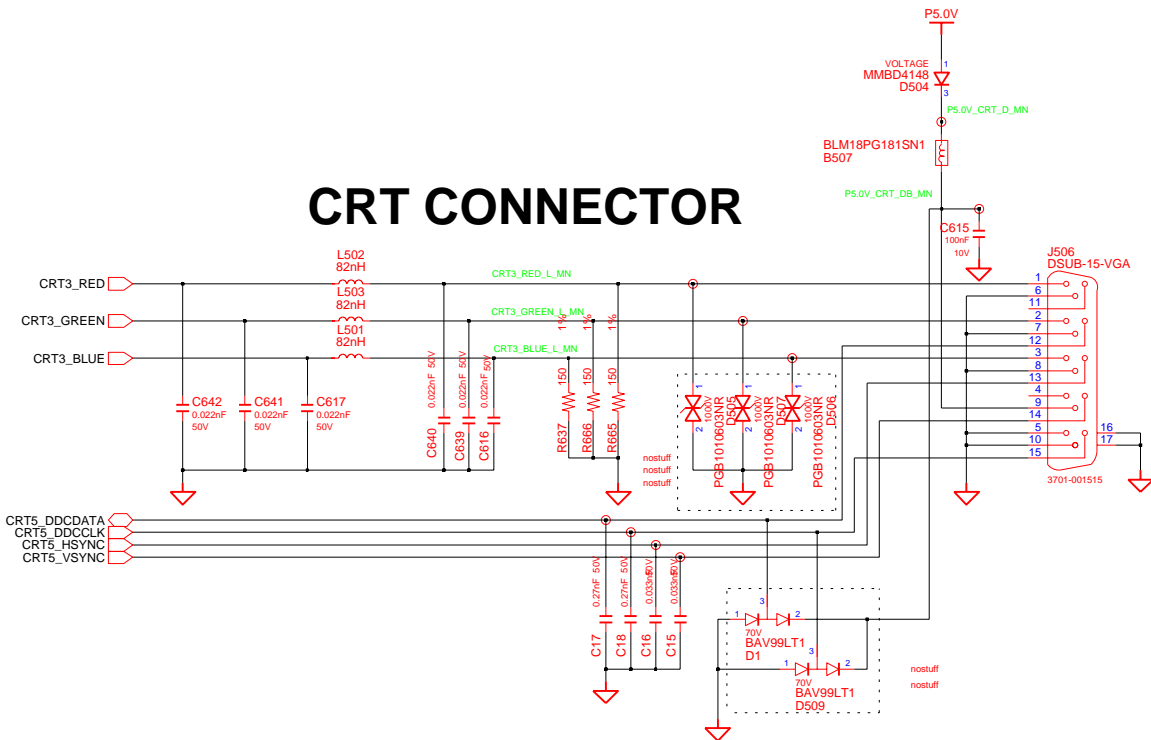
DRAWN	SUN XIAO,	DATE	8/12/2006	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS PART NO. BA41-01213A
CHECK	WU SHIJIANG,	DEV. STEP	PR		SPI_BIOS_ROM	
APPROVAL	BC LEE,	REV	1.0		SPI_BIOS_ROM	
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	25 OF 51	

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CRT



CRT CONNECTOR



Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

DESIGN	SUN XIAO,	DATE	01/08/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	GRAPHICS_IF		
APPROVAL	BC LEE,	REV	1.0	CRT	PART NO.	BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	26	OF 51

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HDMI Level Shifter for Int. Graphic only

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew rate
0	0	0	450mV	0dB	0dB
0	0	1	490mV	0dB	-3dB
0	1	0	450mV	0dB	-3dB
0	1	1	460mV	0dB	-4dB
1	0	0	340mV	0dB	0dB
1	0	1	400mV	2dB	0dB
1	1	0	400mV	2dB	0dB
1	1	1	420mV	0dB	0dB

PC1	PC0
00	9dB
01	4dB
10	12dB
11	0dB

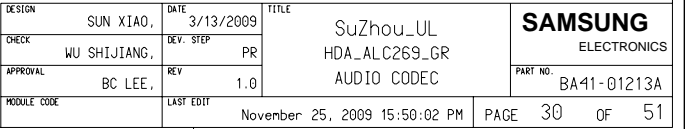
EQ_1	EQ_0	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB

Internal Default Value

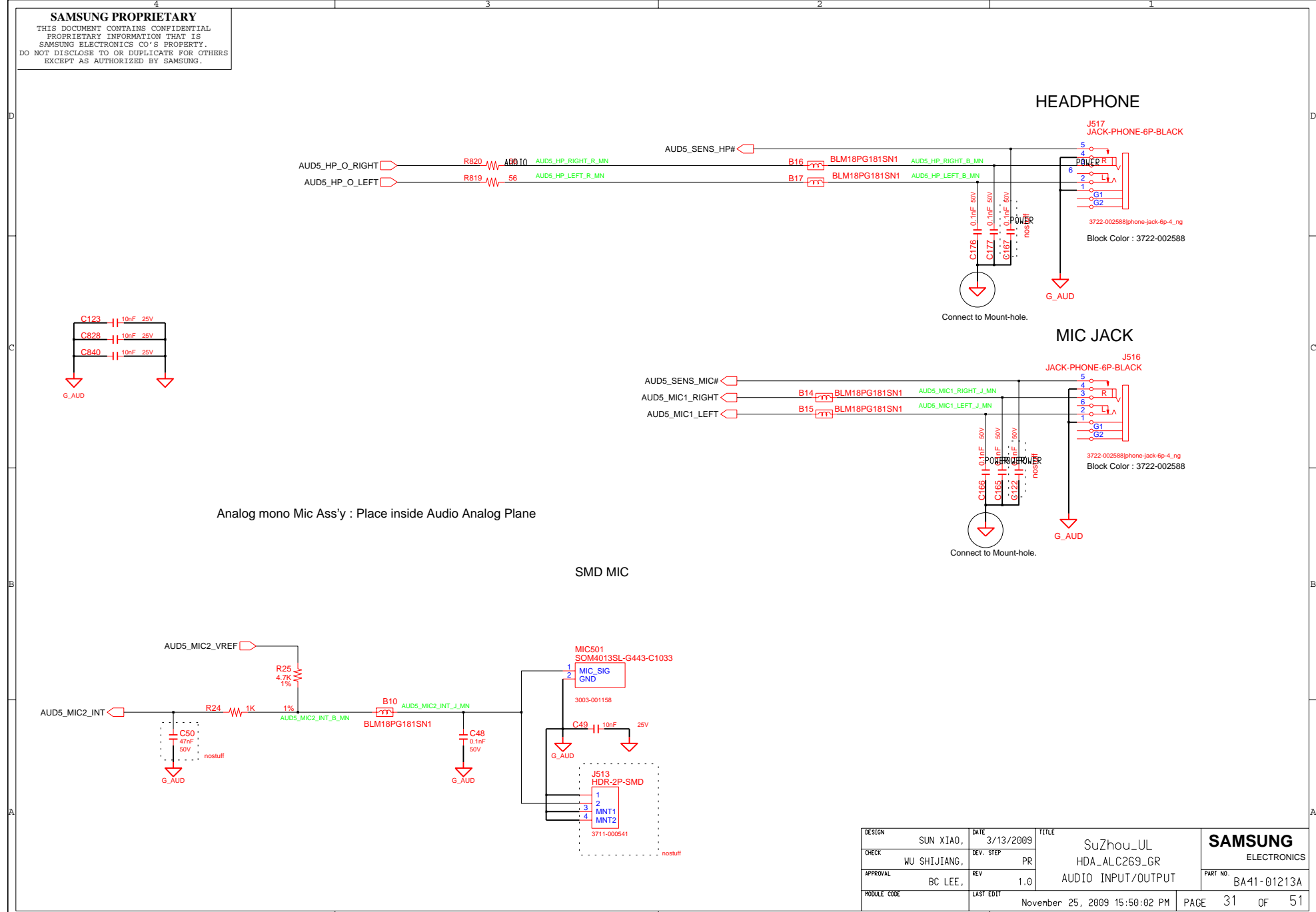
HDMI Level Shifter	REXT(Pin6)	PC1_CG0(Pin3)	PC1_CG1(Pin4)	RT_EN#_CG2(Pin10)	NC_EQ_0(Pin34)	NC_EQ_1(Pin35)	Note
PS8101	499 phm	stuff	nostuff	nostuff	NC	NC	
ASM1442	3.4K(3.24~3.3K)	nostuff	nostuff	nostuff	nostuff	nostuff	Internal PUPD exist CGs nostuff is 450mV swing

DESIGN	SUN XIAO,	DATE	9/14/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	HDMI LEVEL SHIFTER	PART NO.	BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	29	OF 51

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



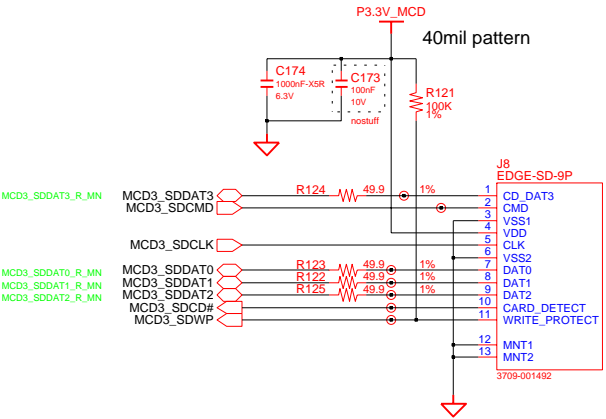
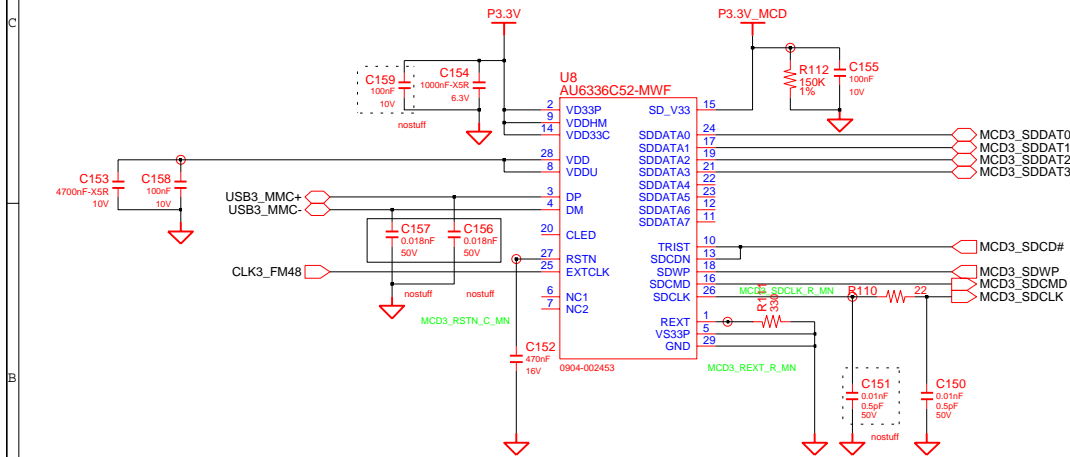
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3 IN 1

P3.3V_MCD distance between R5U880 and socket should be less than 2 inches

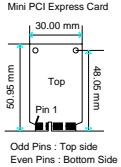
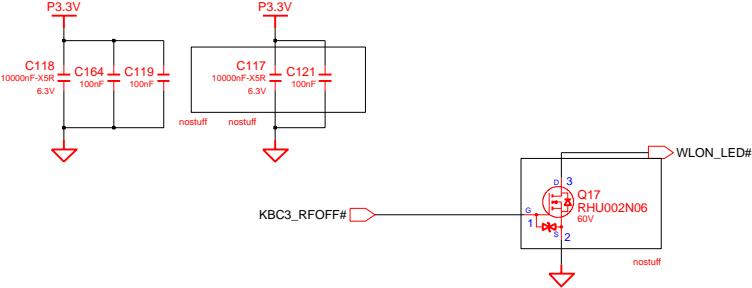
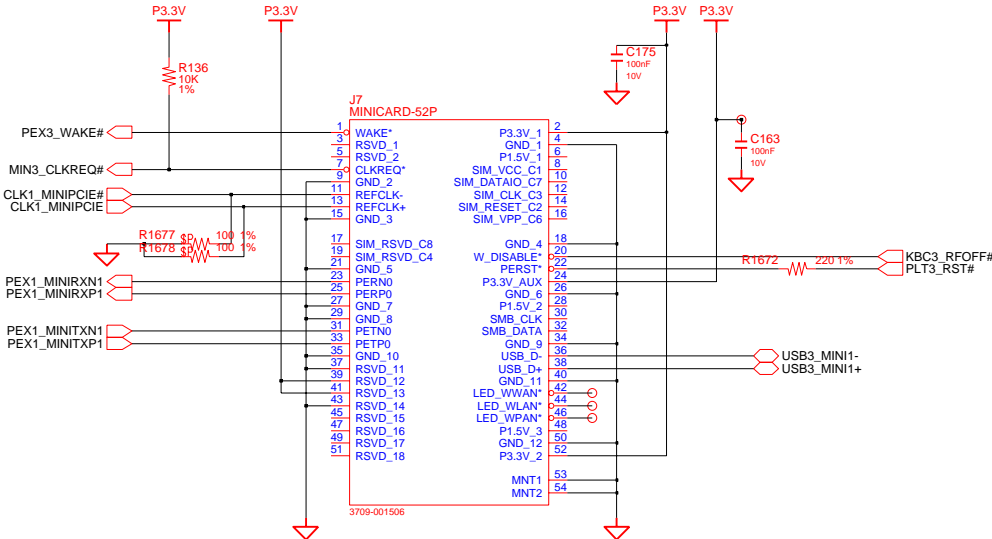


40 mil trace for medica card socket ground

DESIGN	SUN XIAO,	DATE	4/29/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS PART NO. BA41-01213A
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	33 OF 51	

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WLAN, 7mm



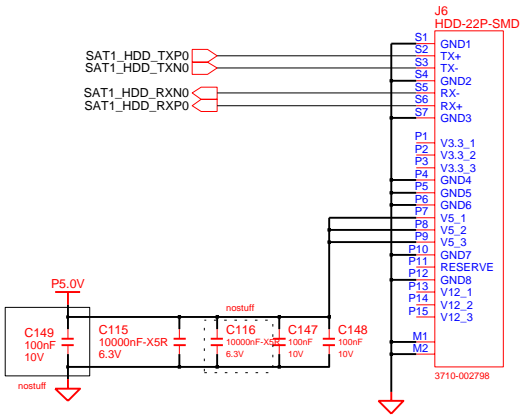
To fix Shirley Peak EMI Issue
Place it at the old rubber area

DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		MINI_PCIE_CONN	
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			
PAGE 34 OF 51						PART NO. BA41-01213A

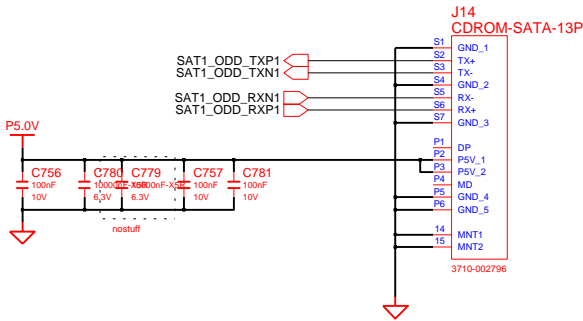
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SATA I/F CONN

SATA HDD CONN

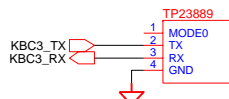
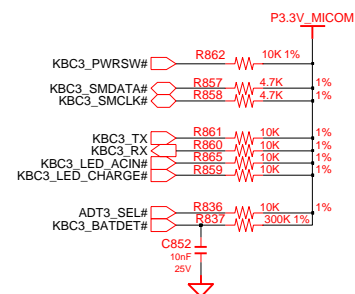
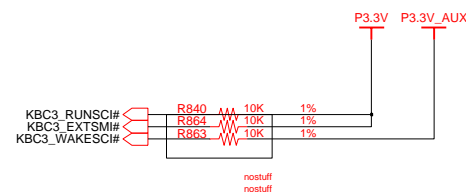


SATA ODD CONN



DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		SATA_DEVICES	
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	35 OF 51	

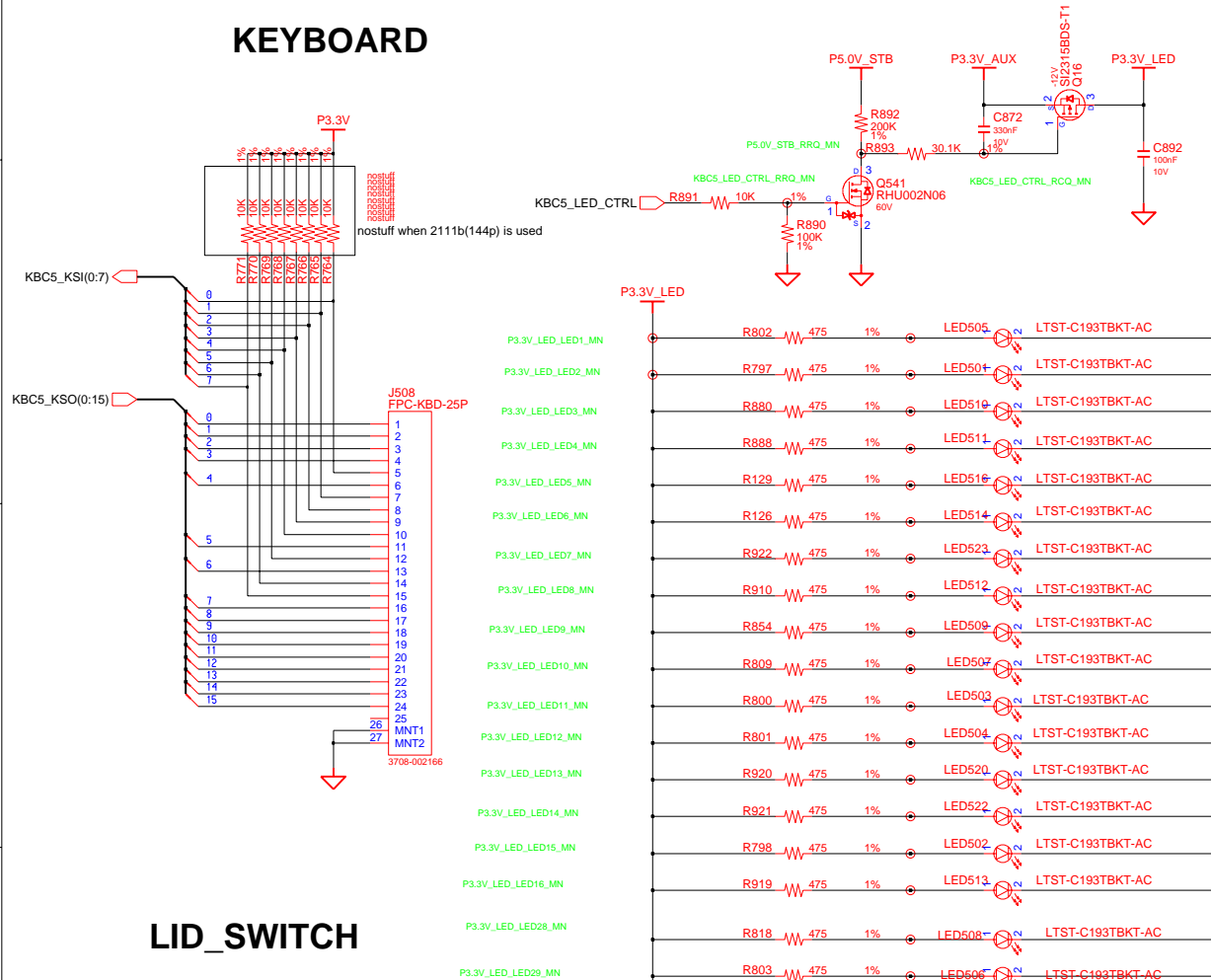
MAIN BOARD (MICOM)

D:/mentor/Suzhou-UI/DDR3/Suzhou-UI-DDR3-PR-091124

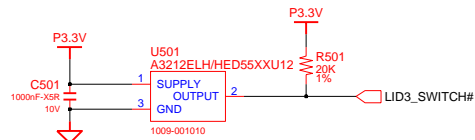
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Micom Glue Logic

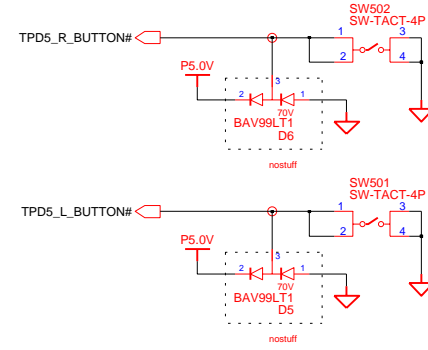
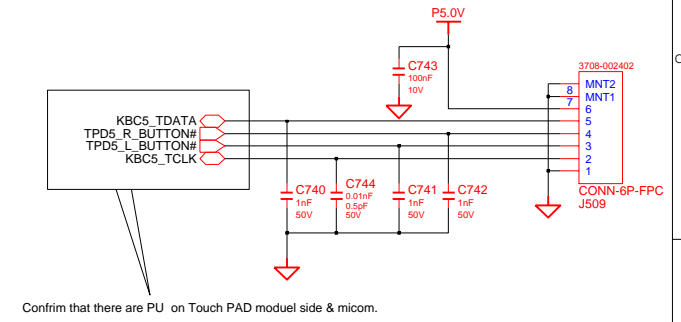
KEYBOARD



LID_SWITCH



TOUCHPAD

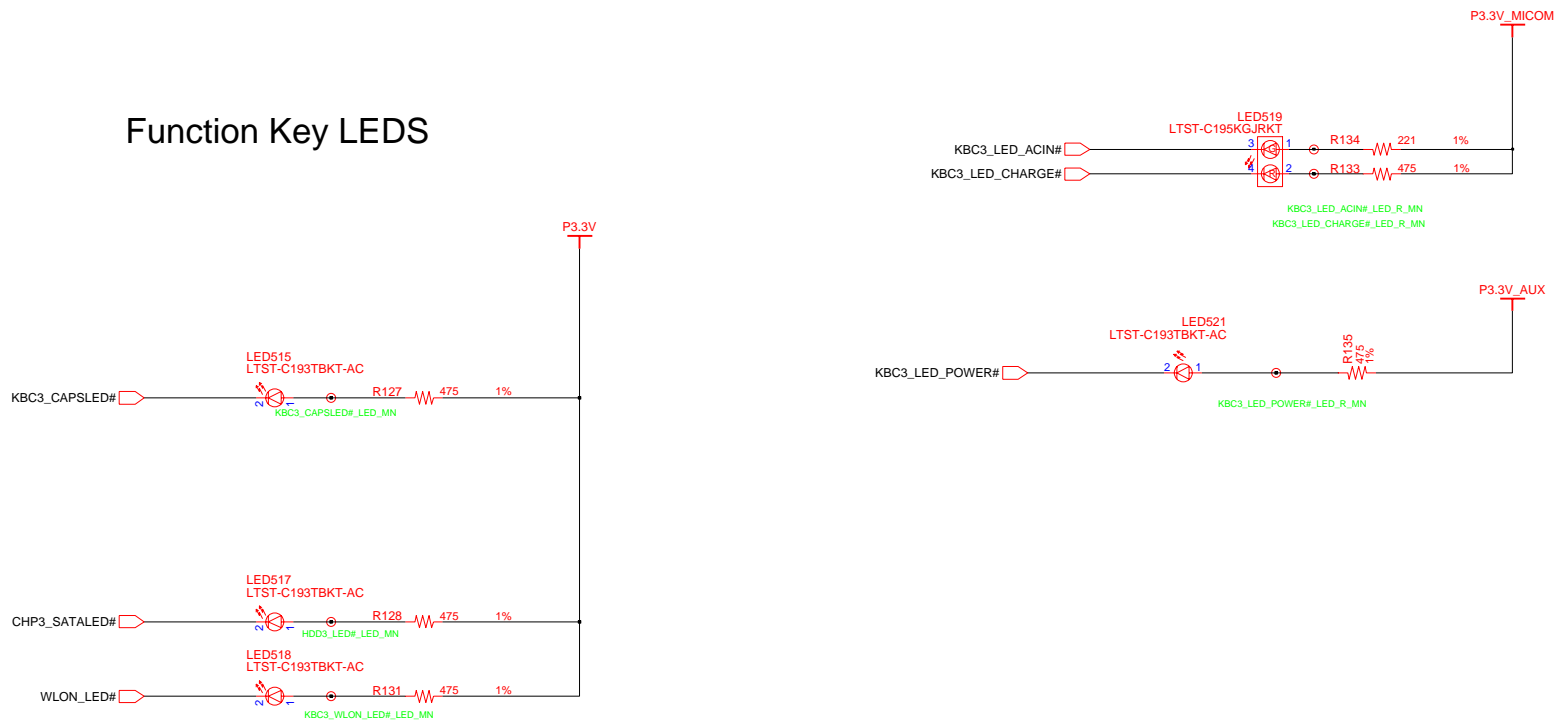


DESIGN	SUN XIAO,	DATE	6/27/2008	TITLE	SuZhou_UL	SAMSUNG
CHECK	WU SHIJIANG,	DEV. STEP	PR			ELECTRONICS
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	37	OF 51

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LED SWITCH LOGIC

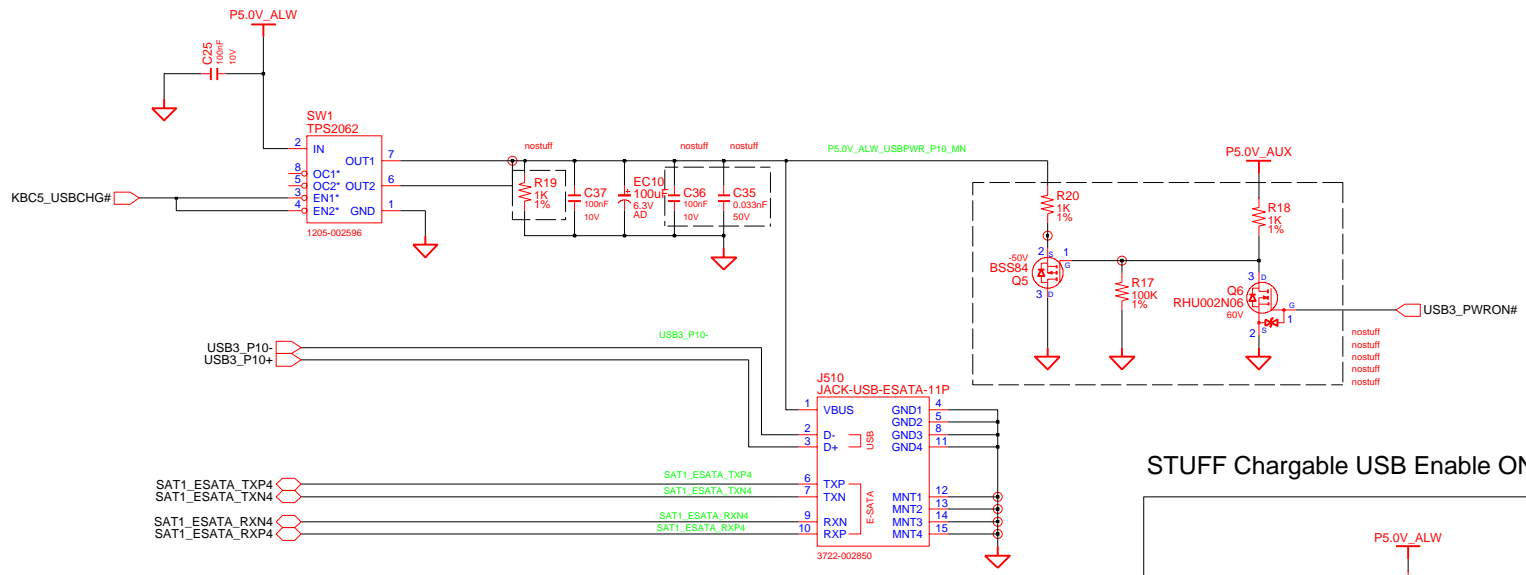
Function Key LEDs



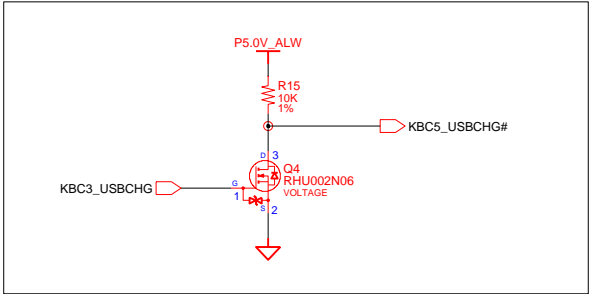
DRAWN	SUN XIAO,	DATE	8/12/2006	TITLE	SuZhou_UL	SAMSUNG
CHECK	WU SHUIJANG,	REV. STEP	PR	LED_Switch	LED_Switch	ELECTRONICS
APPROVAL	BC LEE,	REV	1.0			PART NO.
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM			BA41-01213A
					PAGE	38 OF 51

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eSATA



STUFF Chargeable USB Enable ONLY



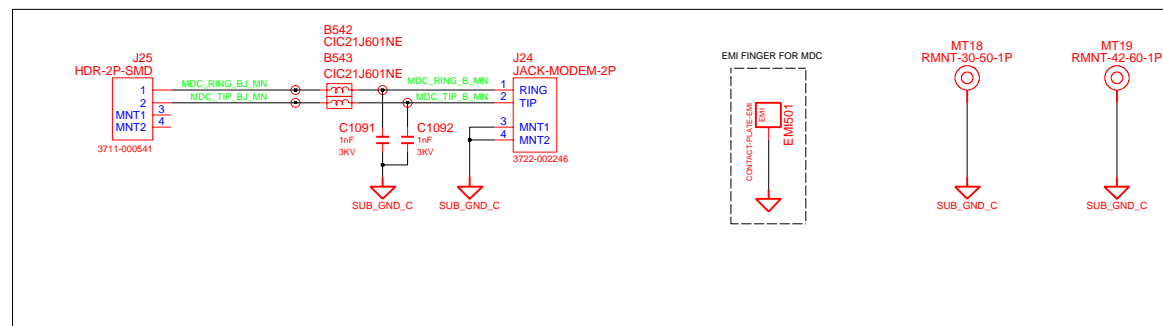
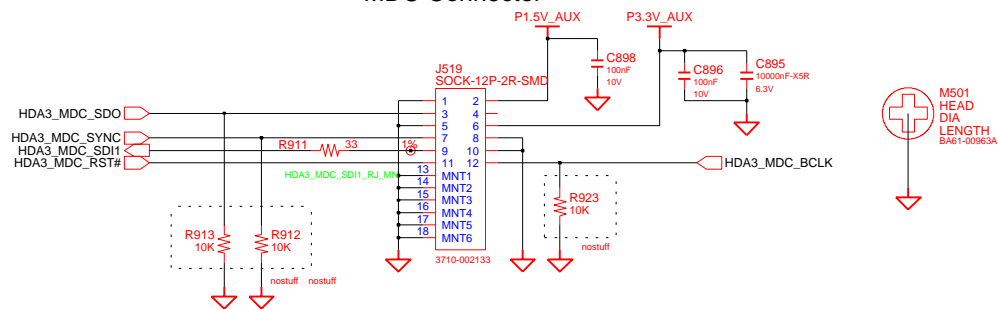
DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN	ESATA	
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	40	OF 51

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MDC

MDC Connector

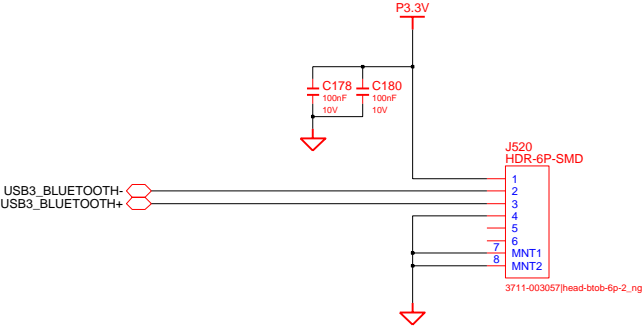


Factory Option

DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	HDA_MODEM		
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	41	OF 51

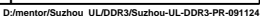
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Bluetooth Interface

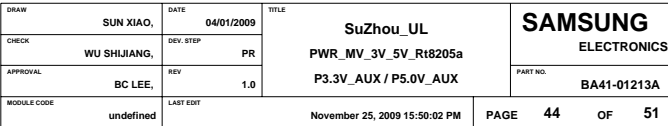


DESIGN	SUN XIAO,	DATE	6/6/2008	SuZhou_UL USB_DEVICES		SAMSUNG ELECTRONICS	
CHECK	WU SHIJIANG,	DEV. STEP	PR				
APPROVAL	BC LEE,	REV	1.0				
MODULE CODE		LAST EDIT		November 25, 2009 15:50:02 PM		PAGE	42 OF 51

CHARGER & POWER MANAGEMENT

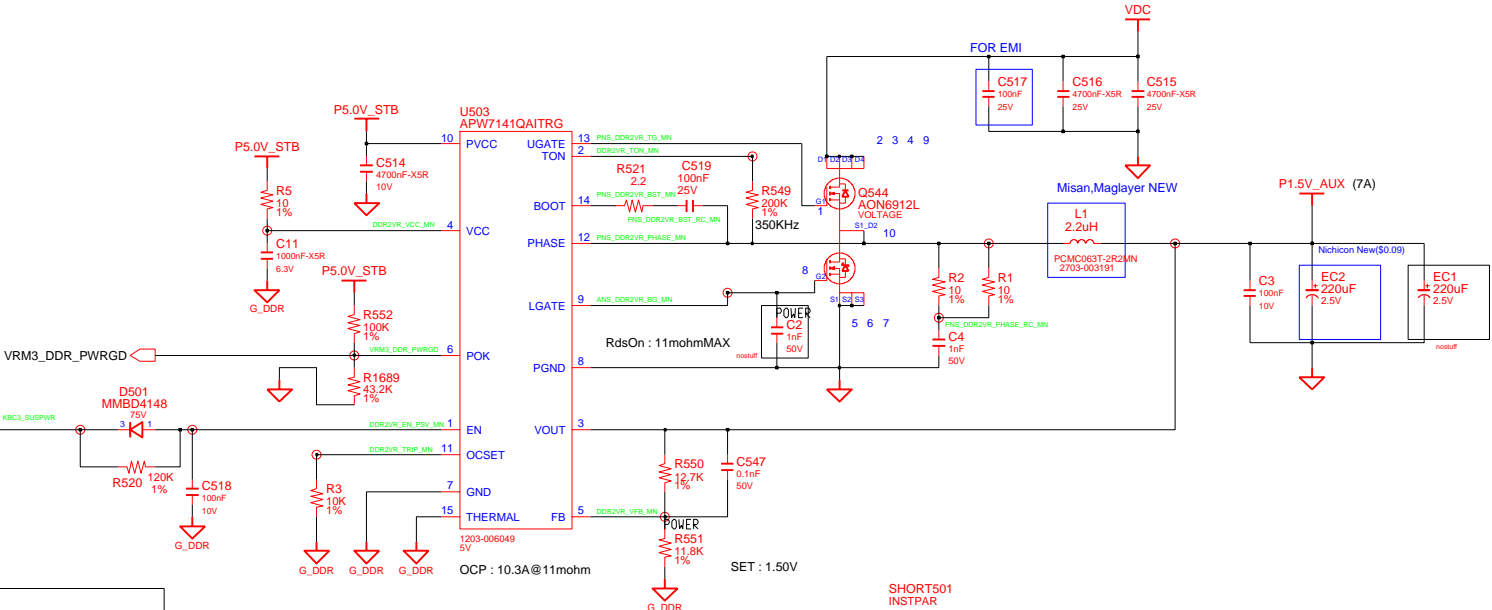


P3.3V_AUX & P5.0V_AUX

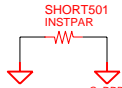
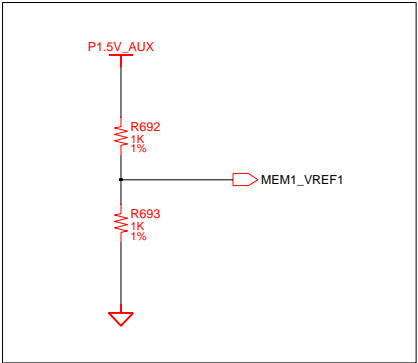


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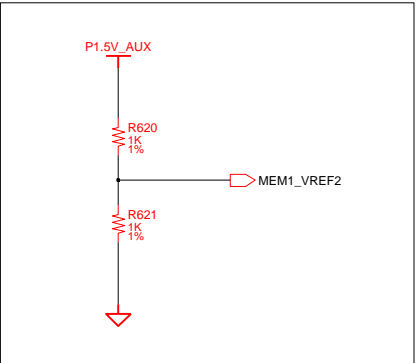
DDR3 Power



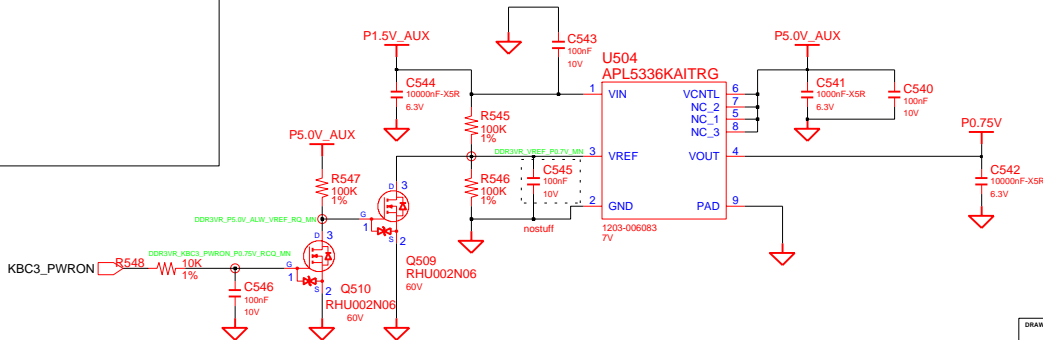
PLEASE PLACE CLOSE TO MCH



PLEASE PLACE CLOSE TO SODIMM



DDR3 VTT(0.75V)

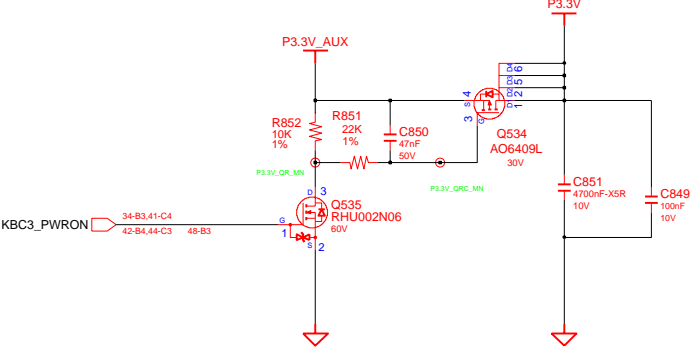


DRAW	SUN XIAO,	DATE	03/13/2009	TITLE	SuZhou_UL	SAMSUNG
CHECK	WU SHIJUANG,	REV. STEP	PR	PWR_MV_Memory_Rt8207	DDR3 POWER (P1.5V_AUX)	ELECTRONICS
APPROVAL	BC LEE,	REV	1.0	November 25, 2009 15:50:02 PM	PAGE 45	OF 51
MODULE CODE	undefined	LAST EDIT				

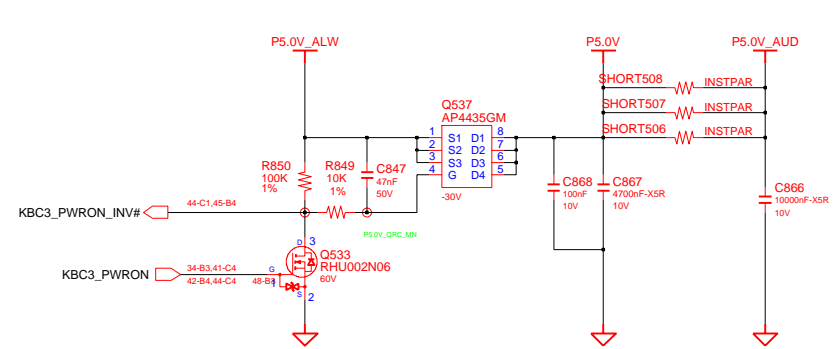
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Switched Power

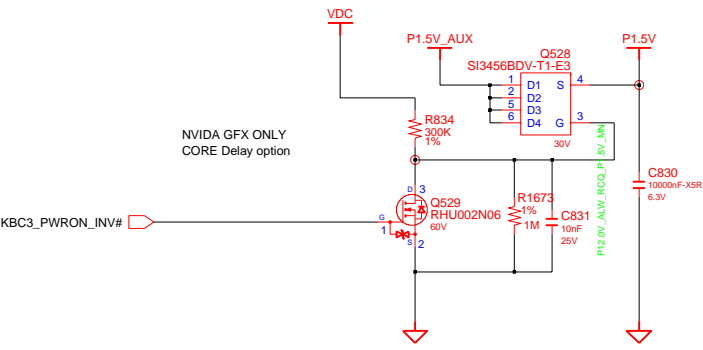
Switched Power On (P3.3V)



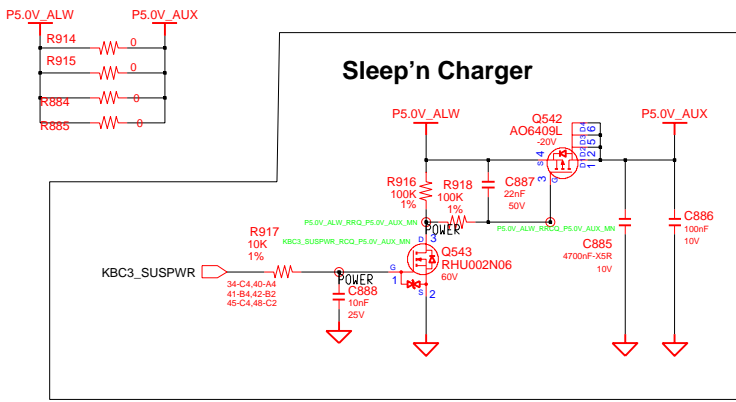
Switched Power On (P5.0V)



Switched Power On (P1.5V)



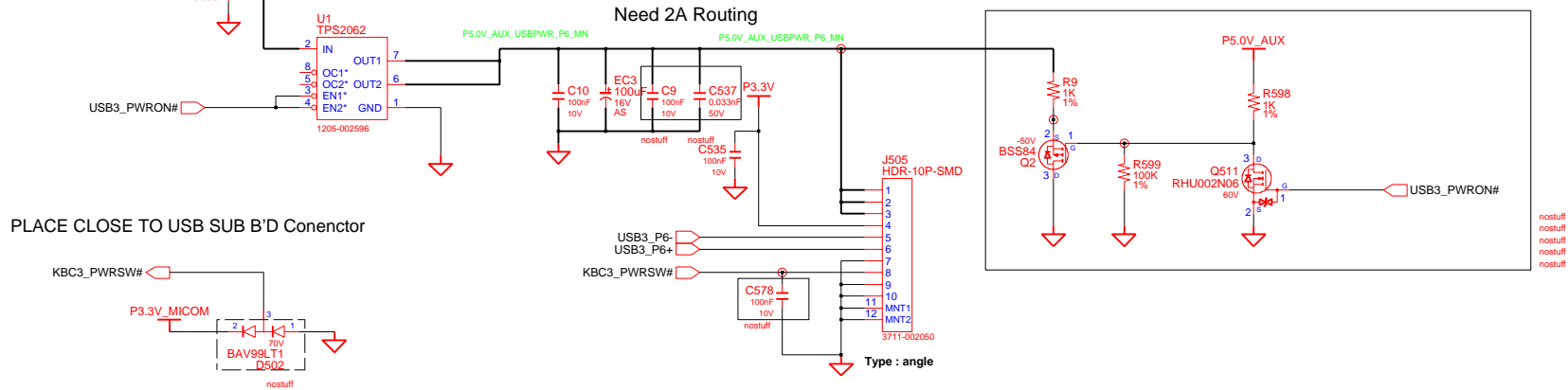
Sleep'n Charger



DRAW	SUN XIAO,	DATE	03/11/2009	TITLE	SuZhou_UL	SAMSUNG
CHECK	WU SHUJIANG,	REV. STEP	PR	PWR_MV_Switched		ELECTRONICS
APPROVAL	BC LEE,	REV	1.0	SWITCHED POWER	PART NO.	BA41-01213A
MODULE CODE		LAST EDIT		November 25, 2009 15:50:02 PM	PAGE	48 OF 51

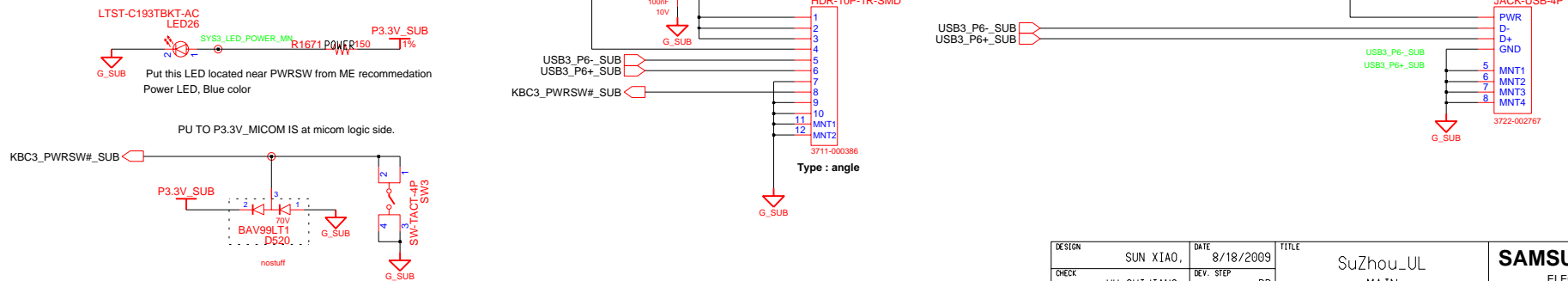
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Main Borad



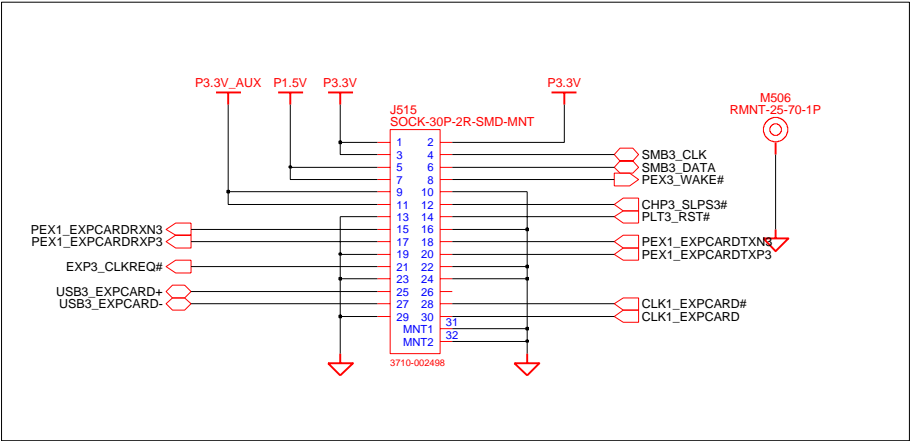
SUB Borad

Power Switch Button



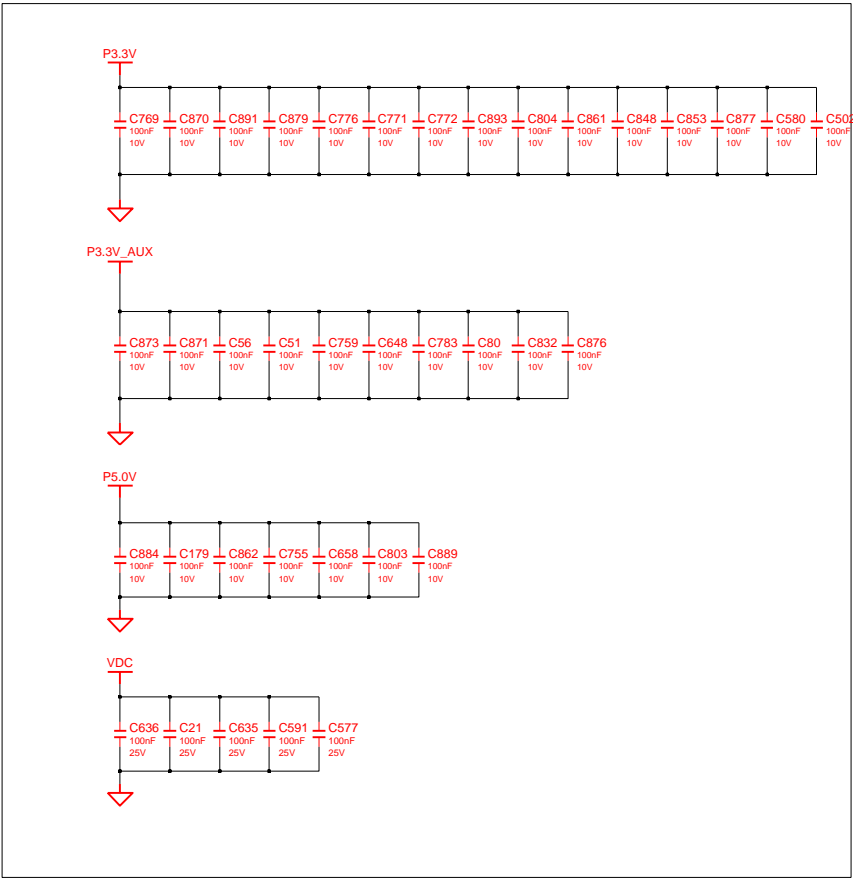
DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	SUB BOARD	PART NO.	BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	50	OF 51

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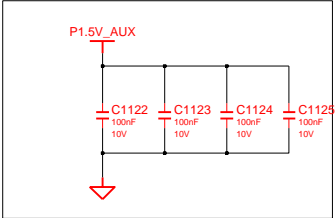
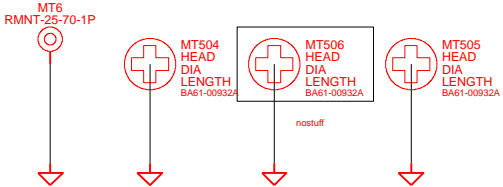
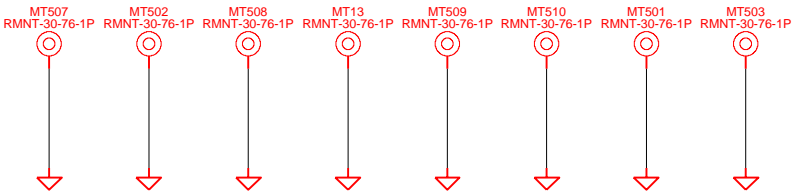


nostuff

nostuff



EMC MODIFY



EMC MODIFY

DESIGN	SUN XIAO,	DATE	9/9/2009	TITLE	SuZhou_UL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN	EXPRESS CARD	
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01213A
MODULE CODE		LAST EDIT	November 25, 2009 15:50:02 PM	PAGE	51	OF 51

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